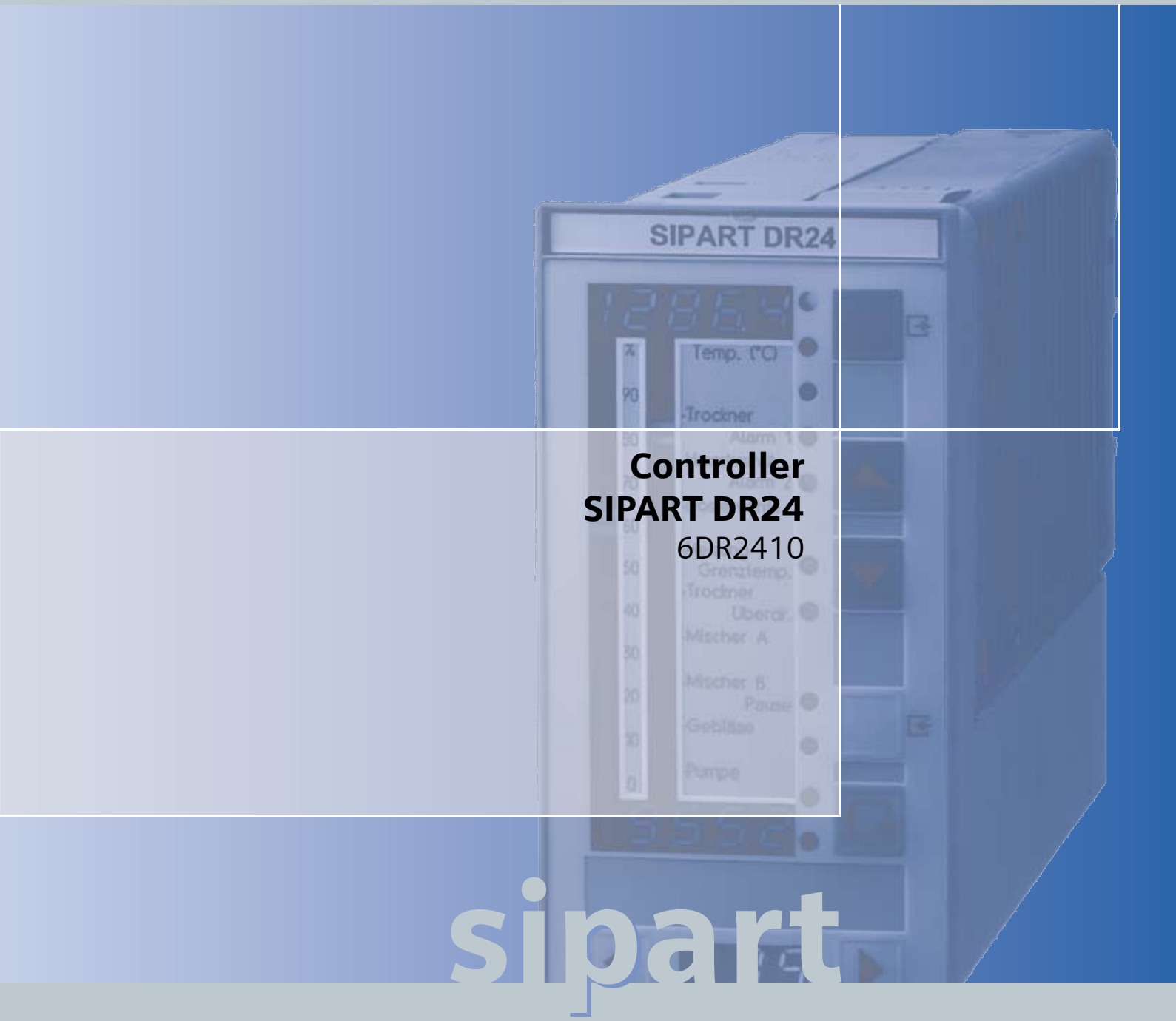
Manual Edition 12/2006



Controller SIPART DR24

6DR2410

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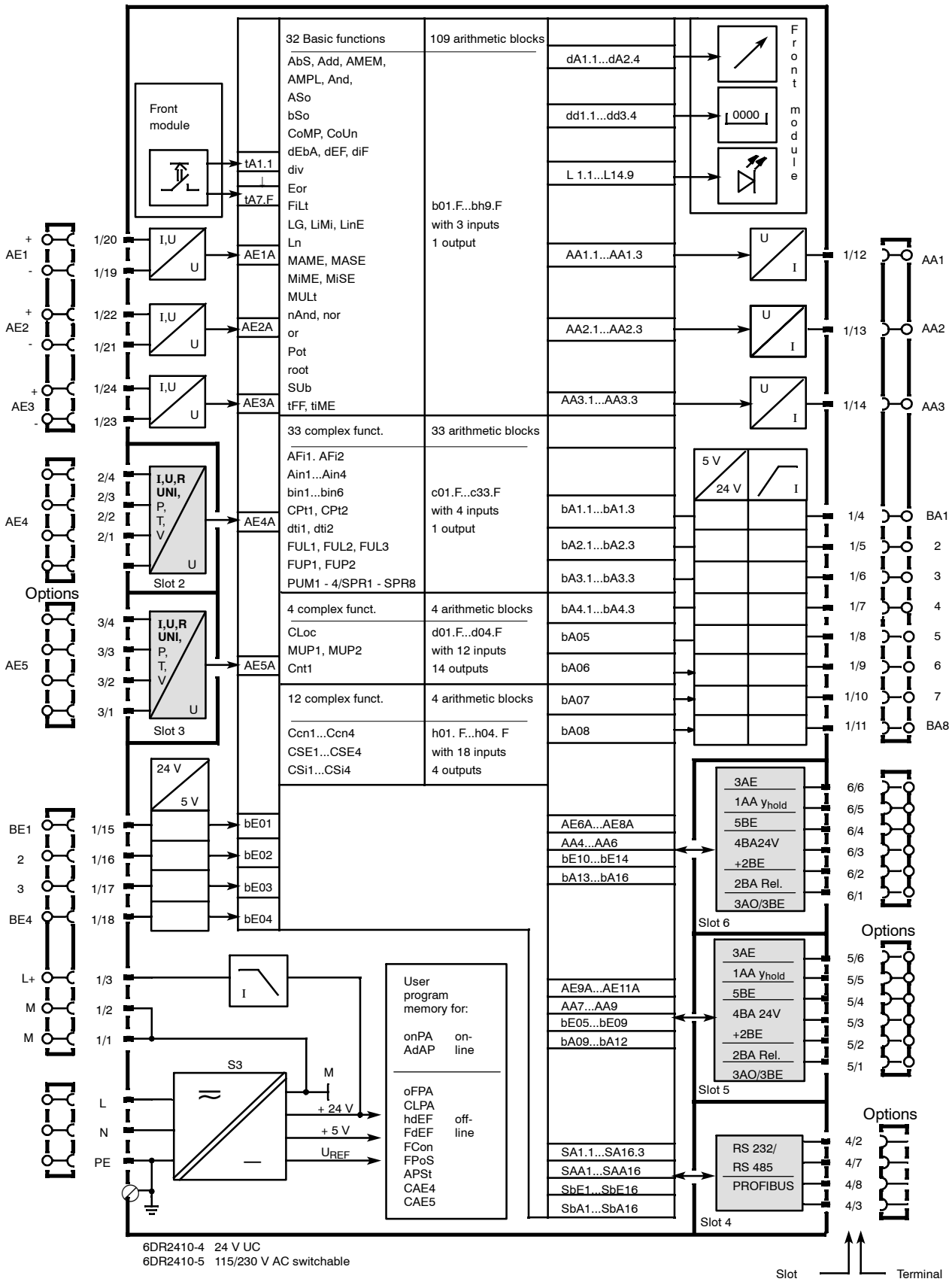
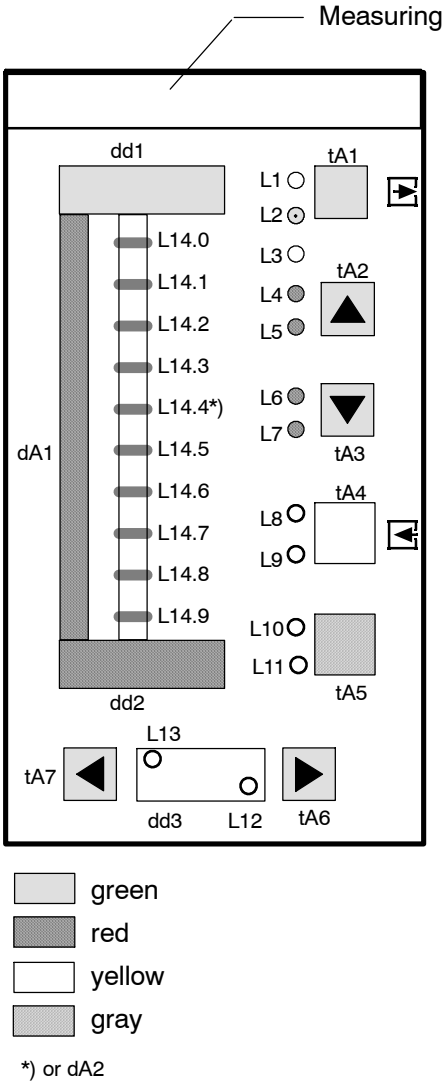
SIPART DR24
6DR2410

Edition 12/2006

Manual

Block diagram





Process operation		Parameterization/configuring
L1	LED green	–
tA1	Key green	Exit key
L2	LED green	Exit LED
L3	LED yellow	–
L4	LED red	–
L5	LED red	–
tA2/3	Key green	Adjustment of the variables shown in the digital display dd1
L6	LED red	–
L7	LED red	–
L8	LED yellow	–
tA4	Key yellow	Enter key
L9	LED yellow	Enter LED
L10	LED green	–
tA5	Key gray	Shift key; start of configuration
L11	LED green	–
L12	LED yellow	–
tA6/7		Adjustment of the variables show in the digital displays dd2 and dd3
L13	LED yellow	–
L14.0 bis L14.9	LEDs green (only as an alternative to digital display dA2)	Striped pattern in configuring
dd1	Digital display green	Parameter value/answer
dd2	Digital display red	Function, parameter name, question
dd3	Didital display yellow	Parameter name
dA1	Analog display red	–
dA2	Analog display green (only as an alternative to L14)	Striped pattern in configuring

Figure 3-1 Connectable control and display elements in the process operation mode and fixed assignment in parameterization/configuring

Classification of safety–related notices

This manual contains notices which you should observe to ensure your own personal safety, as well as to protect the product and connected equipment. These notices are highlighted in the manual by a warning triangle and are marked as follows according to the level of danger:

DANGER

indicates an immenently hazardous situation which, if not avoided, **will** result in death or serious inury.

WARNING

indicates a potentially hazardous situation which, if not avoided, **could** result in death or serious injury.

CAUTION

used with the safety alert symbol indicates a potentially hazardous situation which, if not avoided, **may** result in minor or moderate injury.

CAUTION

used without the safety alert symbol indicates a potentially hazardous situation which, if not avoided, may result in property damage.

NOTICE

indicates a potential situation which, if not avoided, may result in an undesirable result or state.

NOTE

highlights important information on the product, using the product, or part of the documentation that is of particular importance and that will be of benefit to the user.

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Contents

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1 Technical Description

1.1 Safety Notes and Scope of Delivery

WARNING

When operating electrical equipment, certain parts of this equipment automatically carry dangerous voltages. Failure to observe these instructions could therefore lead to serious injury or material damage. Only properly trained and qualified personnel are allowed to work on this equipment. This personnel must be fully conservant with all the warnings and commissioning measures as described in this Manual.
The perfect and safe operation of this equipment is conditional upon proper transport, proper storage, installation and assembly as well as on careful operation and commissioning.

- **Scope of delivery**

  When the controller is delivered the box also contains:

  1 Controller as ordered
  1 three–pin plug at 115/230 V AC or special plug at 24 V UC
  2 Clamps, pluggable
  1 Assembly and installation instructions German/English, order number C79000-M7474-C38

- **Basic equipment**

  The following variants of the SIPART DR24 are available:

Order number	Power supply
6DR2410-4	24 V UC
6DR2410-5	115/230 V AC, switchable

- **Option module**

  Signal converters have separate ordering and delivery items. For handling reasons basic equipment and signal converters which were ordered at the same time may be delivered by separate mail.

- **Documentation**

  This user's guide is available in the following languages:

  English C79000-G7476-C153
  German C79000-G7400-C153

- **Subject to change**

  The manual has been compiled with great care. However, it may be necessary within the scope of product care to make changes to the product and its operation without prior notice which are not contained in this manual. We are not liable for any costs ensuing for this reason.

1.2 Range of Application

The SIPART DR24 is a digitally operating device in the top class range. Its program memory contains a large number of prepared function blocks for calculating, controlling, regulating in chemical engineering processes which the user can implement without programming knowledge and additional tools. Mathematical functions, logical functions, comparison and switching functions, timing functions, memory functions, control functions and a program generator are stored.

All function blocks are freely connectable with each other and with different inputs and outputs of the controller by the software.
The controller can therefore be used to solve a wide range of different problems. A large number of display elements (digital, analog displays, LEDs) and control elements allow display and control of the processes on the front panel.

This controller contains a rugged adaptation procedure for the stored controller components which noticeably simplifies commissioning of even critical control loops. The controller determines the optimized control parameters independently on request without the user being expected to have any prior knowledge of how the control loop may respond.

The SIPART DR24 can operate with up to 4 independent control loops. Tasks in which it is necessary to use interconnected control equipment (e.g. cascaded control, cascaded ratio controls or override controls) can therefore be performed with one controller.

The extensive hardware equipment of the controller allows its universal application and provides a large number of interfaces to the control loop.

The controller can be connected to master systems through a pluggable serial interface (RS 232/RS 485 or PROFIBUS DP) or operated and monitored centrally by a Personal Computer.

1.3 Design (Hardware) Software

The SIPART DR24 has a modular design and is therefore service friendly and easy to convert and retrofit. Other signal converters can be installed in the generously equipped, fully functional standard controller to expand the range of application. These modules are installed in slots at the back of the closed device (Figure 1–2, page 10).

The standard controller consists of

– the front module with the control and display elements
– the main board with CPU and terminal strips
– the plastic housing with an interface board
– the power supply unit.

The electrical connections between the modules are made by an interface board screwed into the housing. The main board is pushed into rear slot 1 and locked. It holds a 10–pin and a 14–pin terminal strip to which all inputs and outputs of the standard controller are connected. Five other slots can be equipped with option modules if the number of terminals to the process available in the standard controller are not sufficient for the planned task.

The basic device always has three permanently installed analog inputs (AE) with electronic potential isolation which can be wired alternatively with standardized voltage signals (0/0.2 to 1 V or 0/2 to 10 V) or current signals (0/4 to 20 mA). There are also four digital inputs (BE, 0/24 V) and eight digital outputs (BA, 0/24 V, 50 mA) which can be used for different functions depending on the configuration.

The SIPART DR24 also has three analog outputs which can all supply a current signal from 0 to 20 mA or 4 to 20 mA and be assigned to different variables.
A short–circuit–proof L+–output (DC 24 V, 100 mA) is available for supplying transmitters.

The power supply unit is located in a fully enclosed metal casing and is screwed tightly to the plastic housing of the controller.

Many applications can be implemented with the three permanently available analog inputs of the standard controller alone. Two additional input modules can be inserted in slots 2 and 3 for complex jobs or for the connection of other input signals. These input modules are available in addition to for processing normalized current and voltage signals for the direct connection of resistance thermometers Pt100 and all common thermocouples and resistance sensors or potentiometers. In addition a module with three analog inputs (equipment as in the standard controller) can be inserted in slots 5 and 6. This increases the number of inputs to a total of 11.

Slot 4 serves to accommodate an interface module (SES) with V.28 point-to-point output or SIPART bus interface for serial communication with a master system. A PROFIBUS interface module can be equipped optionally here.

The slots 5 and 6 can accommodate signal converters of different functions and can be equipped optionally with modules for expanding digital inputs or digital outputs.

Following assemblies are possible:

2 relays
4 digital outputs/2 digital inputs
5 digital inputs
3 analog outputs/3 digital inputs
1 analog output with digital fault output (y_{hold}function) with remote supply
3 analog inputs

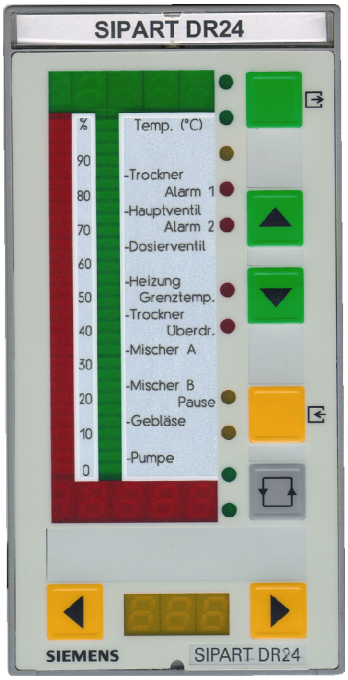


Figure 1–1 Front view of the SIPART DR24

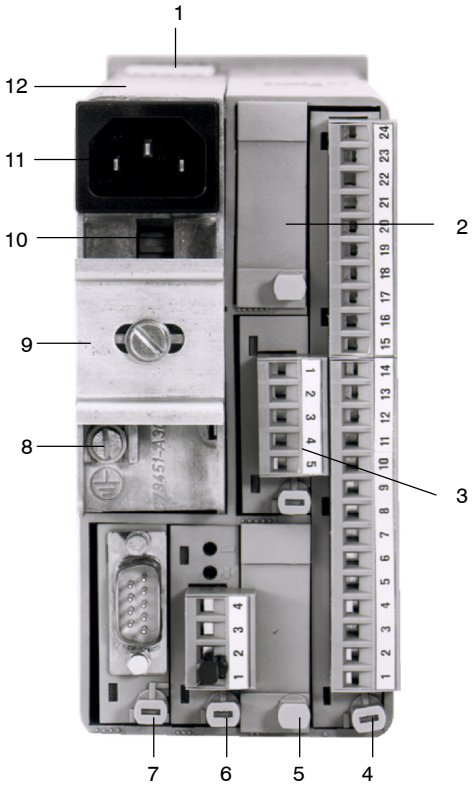


Figure 1–2 Rear view of the SIPART DR24

Legend:
2. PE conductor contact spring
3. Slot 6
4. Slot 5
5. Slot 1 (main board)
6. Slot 2
7. Slot 3
8. Slot 4 (SES: RS 232/ RS 485, Profibus DP)
9. Grounding screw
10. DIN rail (DIN rail delivered with interface relays)
11. Selection switch Mains voltage
12. Mains plug
13. Power supply unit

1.4 Function Principle

1.4.1 Standard Controller

The standard controller consists of three function blocks:

- Power supply unit
- Front module
- Main board

Power supply unit

Primary clocked power supply unit with high efficiency for AC 115/230 V (switchable) or for UC 24 V. It generates the secondary internal supply voltages +24 V and +5 V from the power supply. The metal body is mounted on PE conductors (protection class I). The power supply and internal supply voltages are isolated from each other by safe separation by a protective shield. The internal supply voltages are functional extra–low voltages due to overvoltage cutoff in the event of an error. Since no further voltages are generated in the controller, these statements apply for all field signal lines (used standards, see chapter 1.6, page 93). A total of 450 mA are available for the outputs L+, AA and BA due to the design for a high power output.

Front module

The front module contains the control and display elements and the appropriate trigger components for the displays.

All display elements are designed in LED technology which provides a longer service life and higher light density as well as a good viewing angle. The control elements are short–stroke switches with a tangible ”pressure” and high return force. They are actuated by flexible actuators through the cover foil which are designed so that the foil is not subjected to any excess stress.

The SIPART DR24 has a great number of functional variants. The configured buttons and display elements are activated depending on the function in the front module.

There is a foil behind the front foil which can be labeled to suit requirements. In this way the display and control elements can be assigned to the functions.

Main board

The main board contains the field signal conditioning of the standard controller, the CPU (Central Processing Unit) and the connections (through the interface board) to the module slots.

The field signals are fed through protective circuits for external static or dynamic overvoltages and then adapted to the signal levels of the CPU by the appropriate circuits. This adaptation is performed for the analog inputs, the analog outputs and the digital outputs by modern thick–film circuits.

The microcontroller used has integrated AD- and DA converters and operates with 32k battery–backed RAM. The user–specific configuration is stored in an exchangeable user program memory with a serial 4k EEPROM. This makes it possible to plug the user program memory in the new controller to be installed when servicing. This then does not need to be re–configured.

The whole CPU is designed in C–MOS technology. The program of the SIPART DR24 operates with a variable cycle time which depends on the scope of the program (see chapter 1.5.1, page 21).

A process image is generated at the start of every routine. The analog and digital inputs and actuation of the front buttons is included and the process variables received from the serial interface are accepted. All calculations are performed with these input signals according to the stored functions. Then the data are output to the display elements, the analog outputs and the digital outputs as well as storage of the calculated variables on standby for the serial interface transmitter. The interface traffic runs in interrupt mode.

A large number of arithmetic and function blocks is stored in the set value memory of the SIPART DR24. The user programs the controller himself by selecting, connecting and timing the desired functions by configuration. The entire function of the controller results from the combination of the individual function blocks (basic functions, complex functions) and the corresponding input and output circuits. Programming knowledge is not necessary for the settings. All settings are made without an additional programming device at the operating panel of the SIPART DR24 or via the serial interface. The job–specific program written in this way is saved in the non–volatile user program memory.

There are 32 basic function blocks b**.F and a total of 59 complex functions c**.F, d0*.F, h0*.F which can be used with varying frequency.

No function is stored when the controllers are delivered (factory setting, all preset) The displays are not connected. (Flashing message APSt MEM appears after switching on.)

1.4.2 Description of the Option Module

The following option modules are described in this chapter

6DR2800–8A	3 AE module
6DR2800-8J	I/U module
6DR2800-8R	R module
6DR2800-8V	UNI module
6DR2805-8A	Reference point
6DR2805-8J	Measuring range plug
6DR2801-8D	Module with 2 BA (relays)
6DR2801-8E	Module 2 BE and 4 BA
6DR2801-8C	Module with 5 BE
6DR2802-8A	Analog output module with y-hold function
6DR2802-8B	Module with 3AA and 3BE
6DR2803-8P	Serial interface PROFIBUS-DP
6DR2803-8C	Serial interface RS 232/RS 485
6DR2804-8A	4 BA relays
6DR2804-8B	2 BA relays

6DR2800-8A 3 AE module

- Inputs for current and voltage

To expand the analog inputs.

Description of the module and technical data, see chapter 1.6.2, page 95 (Inputs standard controller).

6DR2800-8J I/U module

- Input variables current 0/4 to 20 mA or voltage 0/0.2 to 1 V or 0/2 to 10 V

The input amplifier of the module is designed as a differentiating amplifier with jumperable gain for 0 to 1 V or 0 to 10 V input signal. For current input signals the 49.9 W 0.1 % impedance is switched on by plug–in bridges on the module. The start value 0 mA and 4 mA or 0 V or 0.2 V (2 V) is defined by configuration in the standard controller. The differentiating amplifier is designed for common mode voltages up to 10 V and has a high common mode suppression. As a result it is possible to connect the current inputs in series as for electrical isolation when they have common ground. At voltage inputs this circuit technique makes it possible to suppress the voltage dips on the ground rail by two–pole wiring on non floating voltage supplies. We refer to an electronic potential isolation.

6DR2800-8R R module

- Input for resistance or current transmitter

Potentiometers with rated values of 80 Ω to 1200 Ω can be connected as resistance transmitters. A constant current of Is = 5 mA is fed to the potentiometer wiper. The wiper resistance is therefore not included in the measurement. Resistances are switched parallel to the potentiometer by a slide switch on the module and a rough range selection made. Range start and end are set with the two adjusting pots on the back of the module.

This fine adjustment can be made via the displays on the front module (with the appropriate configuring). For adjustment with a remote measuring device, the analog output can be assigned to the appropriate input.

The external wiring must be changed for resistance transmitters which cannot withstand the 5 mA wiper current or which have a rated resistance > 1 kΩ. The constant current is then not fed through the wiper but through the whole resistance network of the potentiometer. A voltage divider measurement is now made through the wiper. Coarse adjustment is made by a remote parallel resistor to the resistance transmitter.

This module can also be used as a current input with adjustable range start and end. The load is 49.9 Ω and is referred to ground.

6DR2800-8V UNI module

- Direct connection of thermocouple or Pt100 sensors, resistance or mV transmitters

Measured value sensors such as thermocouples (TC), resistance thermometers Pt100 (RTD), resistance transmitters (R) or voltage transmitters in the mV range can be connected directly. The measuring variable is selected by configuring the controller in the HdeF level (AE4/AE5); the range and the other parameters are set in the CAE4/CAE5 menu. The sensor–specific characteristics (linearization) for thermocouples and Pt100 resistance thermometers are stored in the contoller's program memory and are automatically taken into account. No settings need to be made on the module itself.

The signal lines are connected via a plug terminal block with screw terminals. When using thermocouples with internal reference point, this terminal block must be replaced by the terminal 6DR2805-8A. With the measuring range plug 6DR2805–8J in place of the terminal block, the range of the direct input (0/20...100 mV) can be extended to 0/2...10 V or 0/4...20 mA.

The UNI module operates with an AD converter with 18 bit resolution. The measuring inputs and ground of the standard controller are electrically isolated with a permissible common mode voltage of 50 V UC.

6DR2805-8A Reference point

- Terminal with internal reference point for thermocouples

This terminal is used in connection with the UNI module for temperature measuring with thermocouples at an internal reference point. It consists of a temperature sensor which is pre–assembled on a terminal block and plated to avoid mechanical damage.

6DR2805-8J Measuring range plug

- Measuring range plug for current 0/4 to 20 mA or voltage 0/2 to 10 V

The measuring range plug is used in connection with the UNI module to measure current or voltage. The input variable is reduced to 0/20 to 100 mV by a voltage divider or shunt resistors in the measuring range plug.

Loop resistances with 250 Ω or 50 Ω are available optionally at 2 different terminals for 0/4 to 20 mA signals.

The electrical isolation of the UNI module is retained even when the measuring range plug is used.

6DR2801-8D 2 BA relays

- Digital output module with 2 relay contacts

To convert 2 digital outputs to relay contacts up to 35 V UC.

This module is equipped with 2 relays whose switching contacts have potential free outputs. The RC combinations of the spark quenching elements are respectively parallel to the rest and working contacts.

In AC consumers with low power the current flowing through the capacitor of the spark quenching element when the contact is open may interfere (e.g. the hold current of some switching elements is not dropped below). In this case the capacitors (1 μF) must be removed and replaced with low capacitance capacitors.

The 68 V suppressor diodes parallel to the capacitors act additionally to reduce the induced voltage.

WARNING

The relays used on the digital output module are designed for a maximum rating up to UC 35 V. The same applies for the air and creep lines on the circuit board. Higher voltages may therefore only be switched through appropriately approved series connected circuit elements under observance of the technical data and the pertinent safety regulations.

6DR2801-8E Module 2 BE and 4 BA

- Digital signal module with 2 digital inputs and 4 digital outputs

The module serves to extend the digital inputs and digital outputs already existing in the standard controller.

The inputs are designed for the 24 V logic and are non–floating. The functions are assigned to the inputs and outputs by configuration of the controller.

The digital outputs are short–circuit–proof and can drive commercially available relays or the interface relays 6DR2804–8A/8B directly.

6DR2801-8C 5 BE

- Digital input module with 5 digital inputs

The module serves to extend the digital inputs already existing in the standard controller.

The inputs are designed for the 24 V logic and are non–floating. The function is assigned to the input by configuration of the controller.

6DR2802-8A Analog output module with y-hold function

For auxiliary control device function when servicing and for extending the analog outputs AA1 to AA3 existing in the standard controller.

Can be used in slot 5/6, oP5/oP6 = 1 AA must be set in the hdEF structure mode
Start value of the outputs can be set with AA4/AA7 = 0/4 mA in hdEF

The y_{hold} module contains a microprocessor which maintains serial data communication with the processor on the main board through the Rxd/Txd lines. The processor feeds the U/I converter and the CPU fault message output $\overline{St}$ through its analog output. The module can be externally supplied through an auxiliary voltage input which is OR–linked with the controller power supply. The analog output of the module is freely available.

- **y_{hold} function**

  If data communication to the y_{hold} processor is interrupted, the analog output receives its last value. When data communication is restored, the slave processor reads the current variable first. The output current is maintained if:

  - the self–diagnostics of the CPU (see chapter 1.4.3, page 19) respond.
  - the power supply of the SIPART fails and the y_{hold} module is powered externally.
  - all modules except the power supply unit are removed (if the y_{hold} module is not powered externally).
  - the y_{hold} module is removed (Attention: electrostatically sensitive module! Observe the safety precautions!), if it is powered externally (error message on the front module oP. *.6 Err/oP.*.5, see chapter 1.4.3, page 19).

  This makes it possible to carry out all service work up to changing the controller, e.g. in the case of a controller (arithmetic block h0*.F), and to still maintain the controller manipulated variable.
  Handling during module replacement, see chapter 5, page 169.

- **$\overline{St}$ Fault message output**

  This digital output is always high when there is no error and becomes low in the event of an error. It responds when:

  - the self–diagnostics of the CPU (see chapter 1.4.3, page 19) respond.
  - the controller power supply fails,
  - the y_{hold} module is removed,
  - the main board is removed.

6DR2802-8B Module with 3AA and 3BE

To extend the analog outputs (0/4 to 20 mA) and the digital inputs

Can be inserted	in slot 5:	AA4, AA5, AA6	BE5, BE6, BE7
and	in slot 6:	AA7, AA8, AA9	BE10, BE11, BE12

6DR2803-8P Interface PROFIBUS-DP

The module 6DR2803-8P is a PROFIBUS–DP interface module with RS 485 driver and electrical isolation to the controller. It operates as an intelligent converter module and adapts the private SIPART- to the open PROFIBUS-DP protocol.

This optional card can be inserted in all SIPART–DR controllers in slot 4. The following settings must be made with the appropriate configurations for the serial interface:

– Interface on
– Even parity
– LRC without
– Baud rate 9600
– Parameters/process values writable (as desired)
– Station number according to selection 0 to 125

Make sure that the station number is not assigned double on the bus. The PROFIBUS module serves to connect the SIPART controllers to a master system for operating and monitoring. In addition the parameters and configuring switches of the controller can be read and written. Up to 32 process variables can be selected and read out cyclically by configuration of the PROFIBUS module.

The process data are read out of the controller in a polling procedure with an update time < 300 ms. If the master writes process data to the slave, these become active after a maximum 1 controller cycle.

A technical description including the controller base file (*.GSD) is available for creating a master–slave linking software for interpreting the identifications and useful data from and to the SIPART controller.
The discription and the GSD file can be downloaded from the INTERNET.

www.siemens.com/sipartdr

The programs SIPART S5 DP and S7 DP are offered for certain hardware configurations.

Controller base file and type file, general

The controller base file (GSD file) is necessary for connecting the controllers SIPART DR to any remote systems.
The type file is required at present when connecting to a CPU of the SIMATIC S5/S7.
The DP master connection is parameterized with these files.

6DR2803-8C Serial interface RS 232/RS 485

- Serial interface for RS 232 or RS 485 with electrical isolation

Can be inserted in slot 4.

For connecting the controller SIPART DR24 to a master system for operating and monitoring. All process variables can be sent, the external setpoint, tracking variable, operating modes, parameters and configurations sent and received.

The interface traffic can take place as follows:

RS 232	As point-to-point connection
SIPART Bus	The SIPART bus driver is no longer available. Therefore, please realize multi–couplings via RS 485 or PROFIBUS DP.
RS 485	As a serial data bus with up to 32 users.

The interface module 6DR2803–8C offers electrical isolation between Rxd/Txd and the controller. Switching can be performed between RS 232, SIPART bus and RS 485 with a plug–in bridge.

A detailed technical description of the telegram traffic is available for creating an interface software.

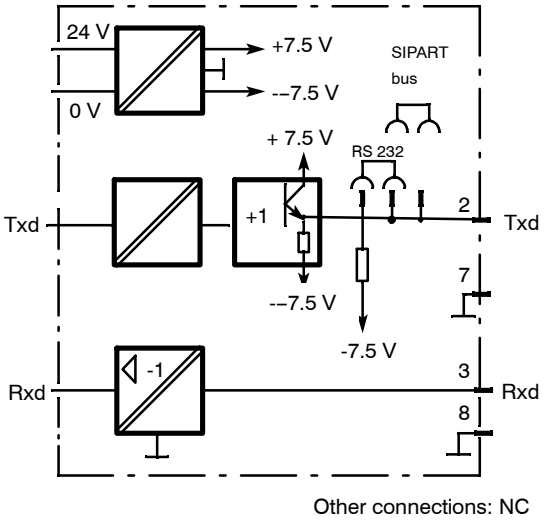


Figure 1–3 Block diagram of serial interface for RS 232/SIPART BUS

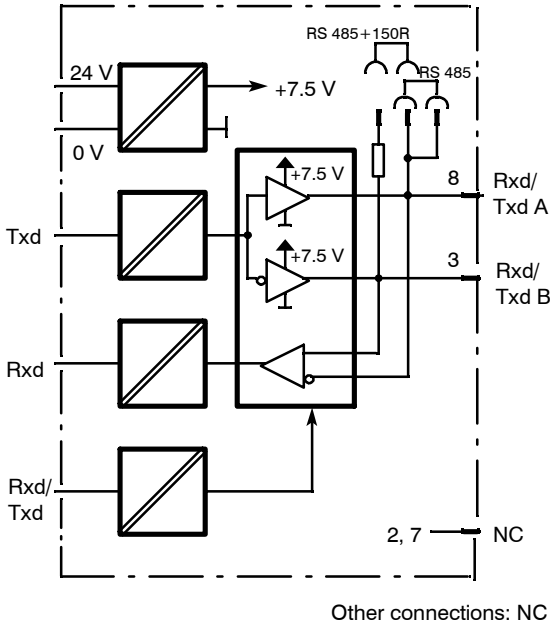


Figure 1–4 Block diagram of serial interface for RS 485

6DR2804-8A 4 BA relays
6DR2804-8B 2 BA relays

- Interface relay module with 2 or 4 relays

To convert 2 or 4 digital outputs to relay contacts up to 230 V UC.

The module can be snapped onto a mounting rail on the back of the controller. The mounting rail is delivered with the interface relay module.

One or two relay modules with 2 relays each are installed depending on the version. Every relay has a switching contact with spark quenching in both switching branches. In AC consumers with a very low power, it is possible that the current flowing (e.g. hold current in contactors) through the spark quenching capacitor (33nF) when the contact is open interferes. In this case they should be replaced by capacitors of the same construction type, voltage strength and lower value.

The switching contact is fed to the plug terminals with 3 poles so that rest and working circuits can be switched. The relays can be controlled directly from the controller's digital outputs by external wiring.

WARNING

The relays used on the interface relay module are designed for a maximum rating of AC 250 V in overvoltage class III and contamination factor 2 according to DIN EN 61010 Part 1.
The same applies for the air and creep lines on the circuit board.
Resonance increases up to twice the rated operating voltage may occur when phase shift motors are controlled. These voltages are available at the open relay contact. Therefore such motors may only be controlled under observance of the technical data and the pertinent safety conditions via approved switching elements.

1.4.3 Self-diagnostics of the CPU

The CPU runs safety diagnostics routines which run after only a reset or cyclically. The CPU is familiar with two different types of reset.

- **Power on reset**

  Power on reset always takes place when the 5 V supply drops below 4.45 V, i.e. the power supply is interrupted for longer than specified in the technical data.
  All parameters and configurations are reloaded from the user program memory into the RAM. At batt = YES (factory setting) the current process variables and status signals are loaded from the battery–backed RAM. At batt = no the startup conditions are fixed (see chapter 1.5.9, page 91).
  At dPon = YES in hdEF the digital displays flash as identification after a power–on reset, acknowledgement is given by the shift key (tA5).

  Flashing is suppressed with dPon = no.

  The fault message source nPon is set to low at power on reset. (See chapter 1.5.5, page 36).

- **Watch dog reset**

  When a watch-dog-reset occurs the parameters and configurations from the user program memory are re-loaded into the RAM. The current process variables and the status signals are read out of the RAM for further processing.
  There are no flashing signals on the front module.

CPU–tESt appears in the digital displays dd1 and dd2 for a maximum 5 s after every reset. Every error detected by the self–diagnostics leads to a flashing error message on the digital displays dd1 and dd2 with defined states of the analog and digital outputs. The fault message output $\overline{St}$ of the y_{hold} module becomes low. The reactions listed in the table are only possible of course (since this is a self–test) if the errors occur in such a way that the appropriate outputs or the front module can still be controlled properly or the outputs themselves are still functioning.

There are other error messages for the input range which suggest defective configurations within this area (see chapter 1.5.6, page 38).
Error messages are also output in the adaptation (see chapter 3.3.2, page 138).
All error messages are shown by flashing digital displays.

1.4.4 Data Storage, User Program Memory

All data are written in the RAM first and then transfered to the user program memory (EEPROM) when returning to the process operation mode (manually or via the SES).
When exchanging the main board, the user memory from the old module can be inserted into the new module.

Writing time

The writing time after leaving the parameterization and configuring modes is up to 30 s. Then the data are stored in a non–volatile memory.

1.5 Functional Description

1.5.1 Basic Structure

The SIPART DR24 is a freely programmable regulation, arithmetic and control unit. It consists of the input section, the functional section and the output section. The functional structure is illustrated in figure 1–5, page 22. The table on page 23 gives an overview of the functions which can be used.

The input section contains the input functions for the 11 analog inputs, the 14 digital inputs, the 7 keys and the input part of the serial interface. (Not all analog and digital inputs can be used at the same time!)

In configuring mode hdEF the function of the slots 5 and 6 and thus the number of BE, BA, AA and AE functions are defined. The input functions convert the process signals (analog and digital inputs) and the manual inputs (keys) into freely connectable data sources.

The output section contains the output functions for the 9 analog outputs, the 16 digital outputs, the 5 displays, the 13 LEDs and the output part of the serial interface.

The output functions convert the freely connectable data sinks into process signals (analog and digital outputs) and visual outputs (displays, LEDs).

The function section is between the input and output sections. It contains 109 arithmetic blocks, in which 32 basic functions can be freely selected and 59 complex functions which can be used with varying frequency. In addition adjustable parameters and a number of constants and fault messages are available for free connection. The freely connectable parameters can be used for the standard functions which have no parameters of their own whereas the complex functions and some of the input and output functions have private (permanently assigned) parameters.

The basic functions have a standardized input/output format, i.e. they have a maximum 3 data sinks (inputs) and 1 data source (output).

The complex functions and the input and output functions have different input/output formats, i.e. the number of data sinks and sources depends on the function depth.
The parameters, constants and fault messages are data sources.

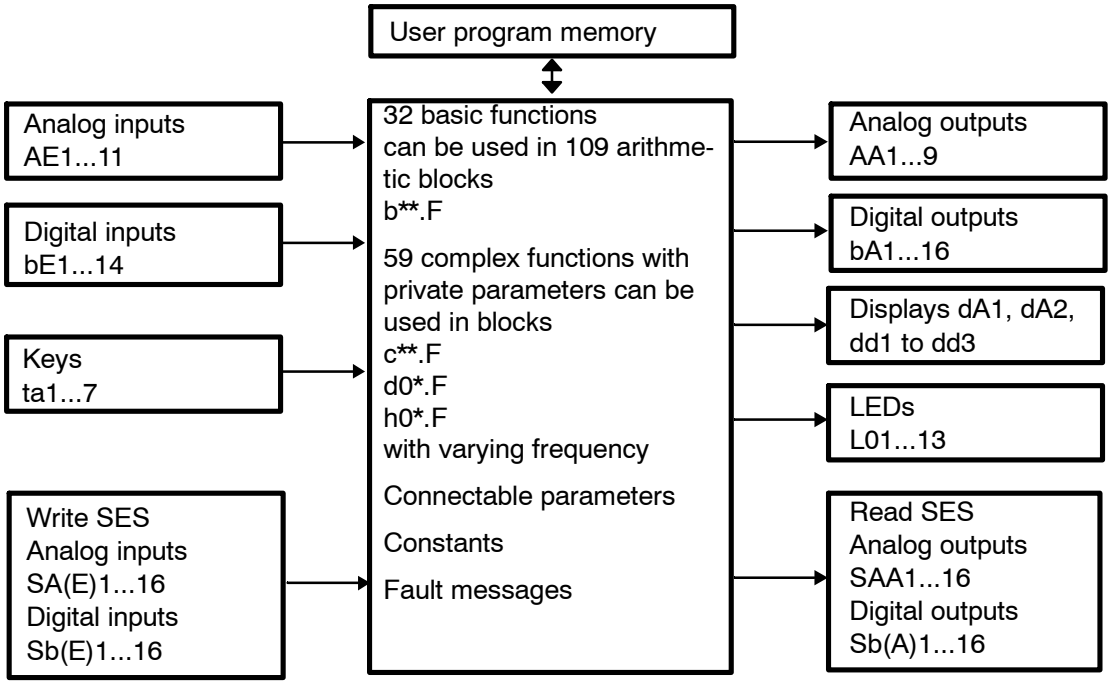
By configuring on the front module, the necessary functions are selected and defined (configuring mode FdEF and hdEF), wired (configuring mode FCon) and timed in the processing (configuring mode FPoS).

Wiring is absolutely free, i.e. any data source can be connected with any data sink. The operating effort is minimized by fading out the data sources and sinks of undefined function blocks and assigning digital data sinks to digital data sources or analog data sinks to analog data sources. In addition the data sinks not absolutely necessary for a function can be defaulted with constants (example: the 3rd input of an adder is defaulted with 0.000).

The connectable parameters and most private parameters can be set during operation in the parameterization mode (online parameters). The other part of the private parameters is set offline in the configuring mode oFPA and CLPA.

The parameter and configuration data are stored in a non-volatile plug-in user program memory with an EEPROM.

The cycle time in online operation depends on the scope of the user program and is a minimum 60 ms. About 2 ms are necessary on average per basic function, and about 5 ms per complex function. The cycle time in offline operation is 100 ms.
Addition of the individual times gives the total cycle time t_c which changes in 10 ms steps.
The current cycle time can be displayed during the lamp test (see chapter 5.1, page 169) by additionally pressing tA1. dd3 shows the cycle time in ms.
On average you can reckon on 80 to 120 ms cycle time.



Operating modes:

Process operation
Parameterization (Online)
AdAP Adaptation
Configuring (Offline)

oFPA	Offline parameters
CAE4	Parameterize UNI-module for AE4
CAE5	Parameterize UNI-module for AE5
CLPA	Clock parameters
hdEF	Define hardware
FdEF	Define functions
FCon	Wire functions
FPoS	Position functions
APSt	Load factory setting (all preset)

Figure 1–5 Block diagram of the SIPART DR24

Functional overview SIPART DR24

b = Basic function, blocks b
c = complex function, blocks c
d = complex function, blocks d
h = complex function, blocks h

● Mathematical functions		Function block
AbS	Absolute value	b
Add	Adder	b
AMPL	Differential amplifier	b
CPt	P/T correction computer	c
div	Divider	b
FUL	Function transmitter (linear)	c
FUP	Function transmitter (parabola)	c
LG	Decadic logarithmer	b
LinE	Linear equation	b
LN	Natural logarithmer	b
MUlt	Multiplier	b
Pot	Exponential function	b
root	Rooter	b
SUb	Subtractor	b

● Logical functions		Function block
And	AND	b
CoUn	Counter	b
dFF	D–flip–flop	b
Eor	EXOR	b
nAnd	NAND	b
nor	NOR	b
or	OR	b
SPR	Split range	c
tFF	T–flip–flop	b
tiME	Timer (monoflop)	b

● Comparison and switching functions		Function block
AMPL	Differential amplifier	b
ASo	Analog switch over	b
bSo	Digital switch over	b
Cnt	Demultiplexer	d
CoMP	Comparator with hysteresis	b
dEbA	Response threshold (dead band)	b
LiMi	Limiter	b
MASE	Maximum selection	b
MiSE	Minimum selection	b
MUP	Measuring point switch over (analog)	d

● Timer functions		Function block
AFi	Adaptive filter	c
Ain	Integrator with analog input	c
bin	Integrator with digital input	c
diF	Differentiator	b
dti	Dead time element	c
FiLt	Filter (low pass)	b
PUM	Pulse width modulator	c
tiME	Timer (monoflop)	b

● Memory functions		Function block
Ain	Integrator with analog input	c
AMEM	Analog memory	b
bin	Integrator with digital input	c
dFF	D–flip–flop	b
MAME	Maximum memory (drag pointer)	b
MiME	Minimum memory (drag pointer)	b
tFF	T–flip–flop	b

● Control functions		Function block
Ccn	K controller	h
CSE	S controller external feed back	h
CSi	S controller internal feed-back	h

● Program transmitter		Function block
CLoc	Clock	d

1.5.2 Input Functions

The following input functions are dealt with in detail in this chapter:

Analog inputs	AE1 to AE11
Digital inputs	BE1 to BE14
Data sinks	bLS, bLPS, bLb
Keys	tA1 to tA7

Analog inputs AE1 to AE11

The analog inputs AE1 to AE3 are located on the basic board and can be jumpered there. Ranges: 1 V, 10 V, 20 mA. (The zero point can be selected via configuring mode hdEF (AE1 to AE11).) The inputs AE4, AE5 are realized with a module card in slots 2 and 3. The inputs AE6 to AE8 are realized with a module in slot 6. The inputs AE9 to AE11 are realized with a module in slot 5. Ranges same as AE1 to AE3.

The A/D converter inputs have a signal range from –5 % to +105 % or as an absolute value –0.05 bis +1.05. If the evaluation of the inputs is to be changed you can switch the basic function “Multiply” (MULt) for weakening or strengthening the basic function and the basic function “Linear equation” (LinE) to hide a range by configuring (see chapter 1.5.6, page 38).

The analog inputs AE***** (*****= 1 to 11) have a mains frequency suppression (configuring level hdEF)

AEFr 50 or 60 Hz

and the transmitter monitor AE1 ↳ to AE11 ↳ as a data source with a threshold at –3 % and 103%. The thresholds have a hysteresis of 1 %. The data source can be switched in FCon. The fault message nAE ↳ is set to low when the values exceed or drop below the limit. This signal is also freely switchable in FCon.

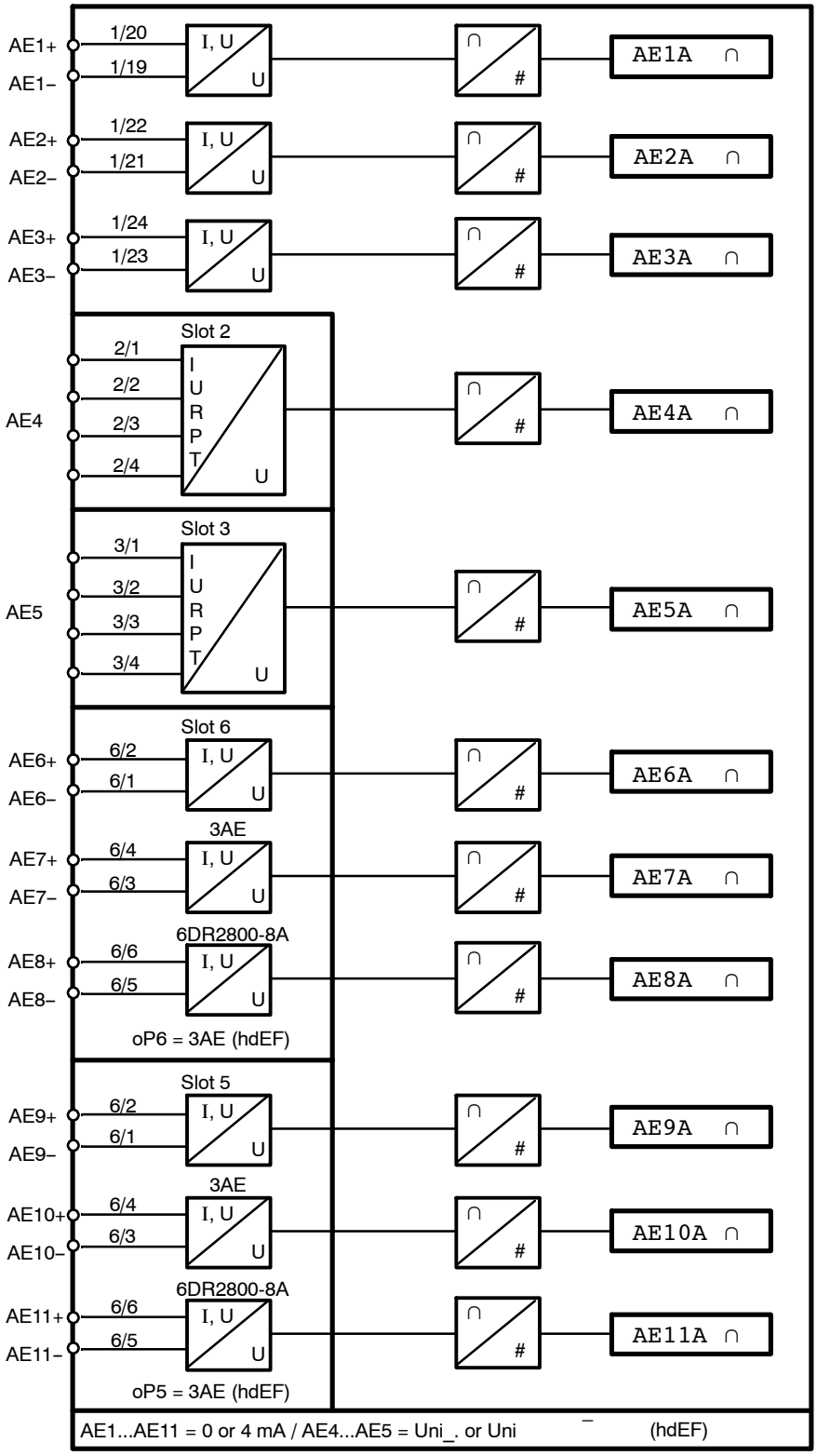


Figure 1–6 Input function analog inputs

Digital inputs BE1 to BE14

The inputs BE1 to BE4 are located on the basic board. BE5 to 9 and 10 to 14 are connected to the module 6DR2801–8C at the slots 5 or 6. The digital output modules 6DR2801–8E also contain another two digital inputs in addition to the outputs so that in this case the two digital inputs BE5/BE6 or BE10/BE11 can be used.
The modules are assigned to the slots in the configuring mode hdEF.

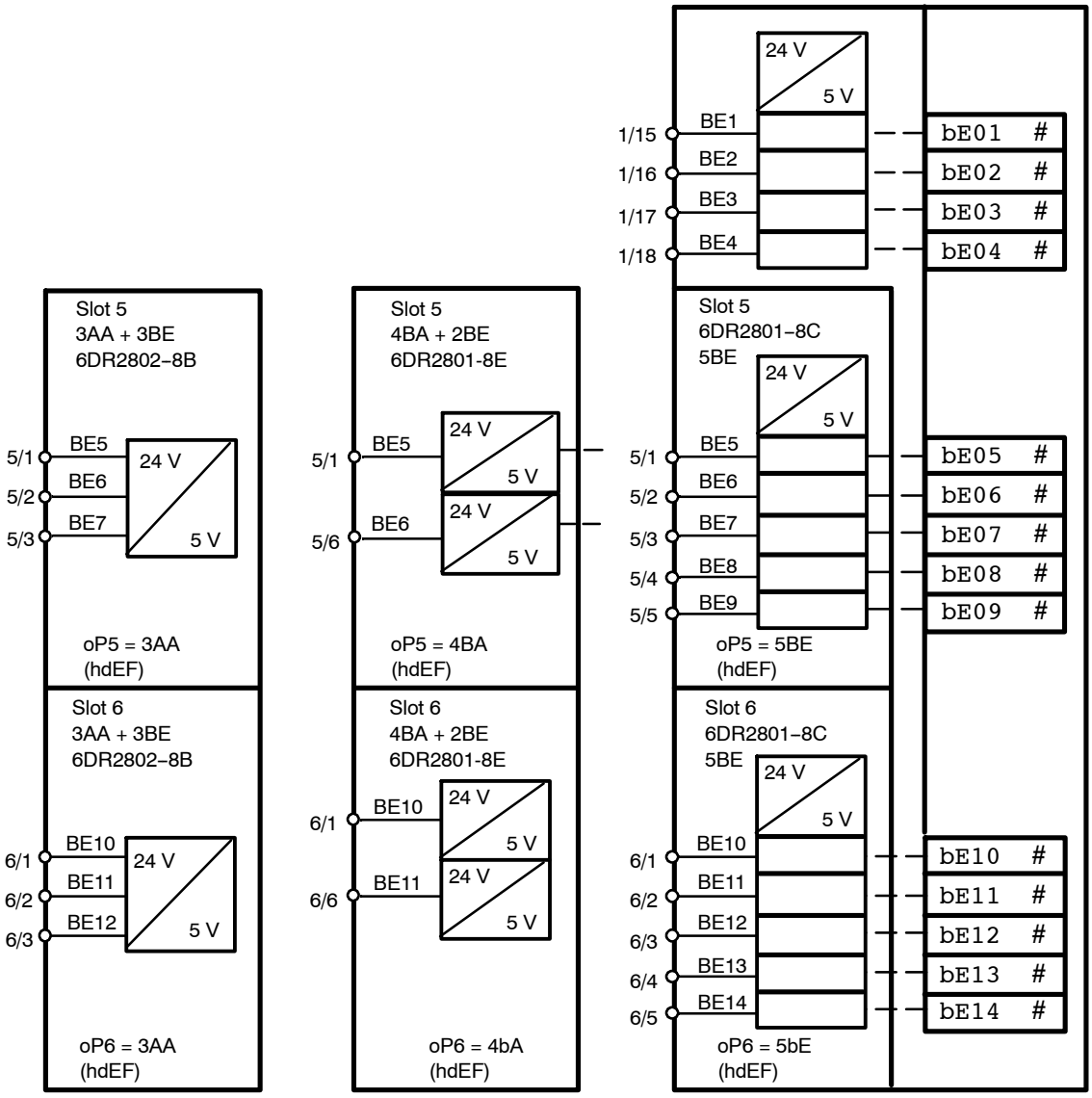


Figure 1–7 Input function digital inputs

Data sinks bLS, bLPS, bLb

These sinks serve to block operation (bLb), the parameter and configuration adjustment (bLPS) or just the configuration adjustment (bLS). At bLPS = high an error message no(dd1) PS(dd3) is displayed when attempting to enter the parameterization mode.

At bLS = high no error message appears but the StrU level in the parameterization preselection is hidden. The sinks bLS, bLPS and bLB can only be switched by the binary inputs BE1 to BE14 (bE** = source) and the SES sources SbE1 to SbE8. When the CB time monitor responds or at Cbt = oFF, the SES sources connected with bLS, bLPS or bLb are set to low. See also chapter 3.3.7, table 3–8, page 157.
The factory setting is low.

Keys tA1 to tA7

The keys (see figure 1–9, page 28) are available as key function tA*.1, tA*.2 or as switching functions tA*.3, tA*.4 or tA*.5, tA*.6 (see figure 1–8, page 28). The keys are provided primarily for incremental adjustment of the complex functions „Integrator with digital input” (bin) or controller inputs $\pm \Delta y$. They can be switched by the control inputs tA*U/tA*M for quadruple applications whereby the status of the switched off outputs Q and $\overline{Q}$ remains unchanged.

The key tA5 has no key output to other operating levels because of the universal function; i.e. tA5.1 and possibly tA5.2 are not available. The outputs Q and $\overline{Q}$ are switched at key 5 with the low edge (release the key). “PS” flashes in dd3 after pressing tA5 continuously for about 5 s. All keys lose their function in the process operating level when the display flashes in dd3.

You can now switch to the other levels (parametering, configuring). See chapter 3.3.1 (page 136), 3.3.2 (page 138) and 3.3, page 135.

When the function tA*.U is assigned „no” in the configuring mode hdEF, the shaded data sources and sinks do not appear in the configuring mode FCon. Since the sink tA*.U is pre–assigned with low, the drawn switch position is active.

Restart conditions

Power on	Q	$\overline{Q}$
bAtt = no	0	1
bAtt = YES	last status	last status

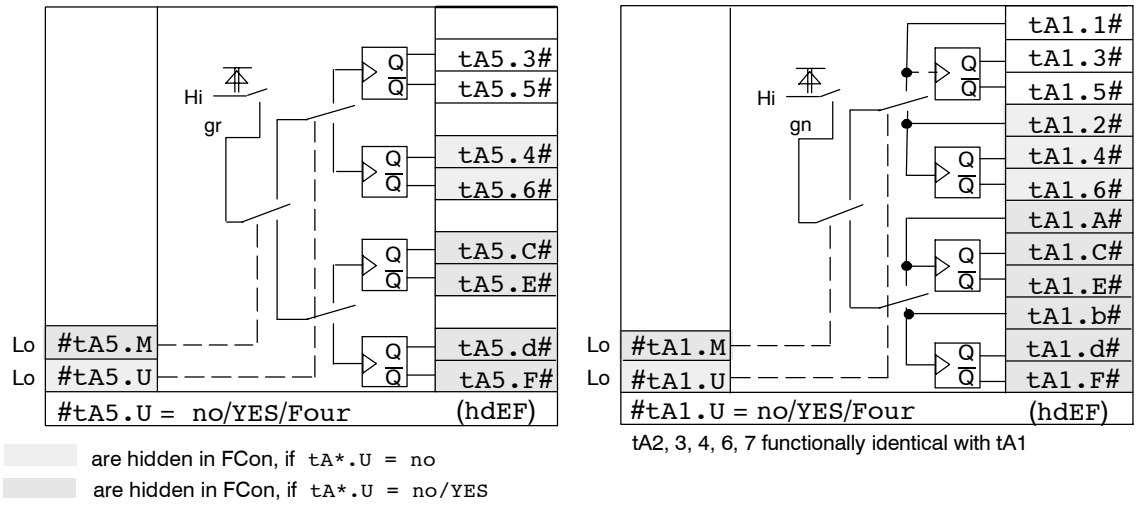


Figure 1–8 Input function keys

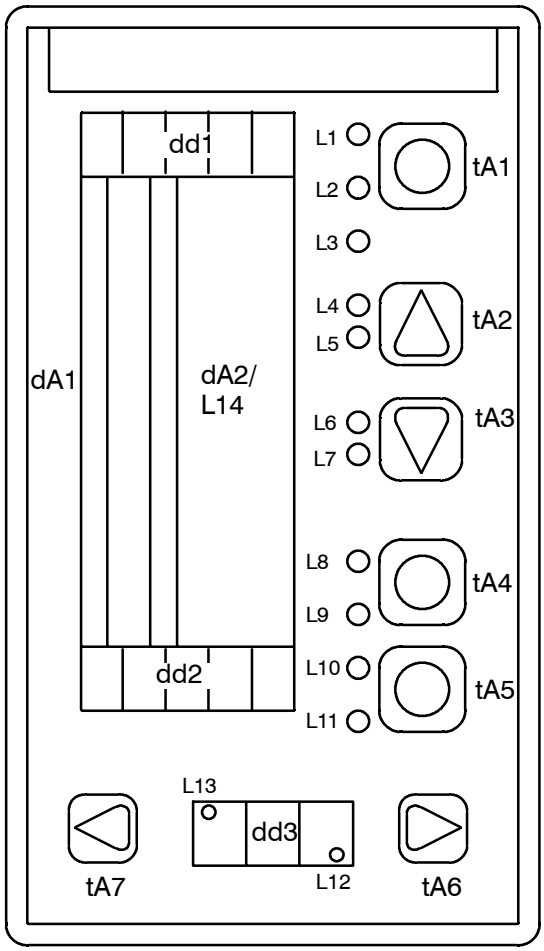


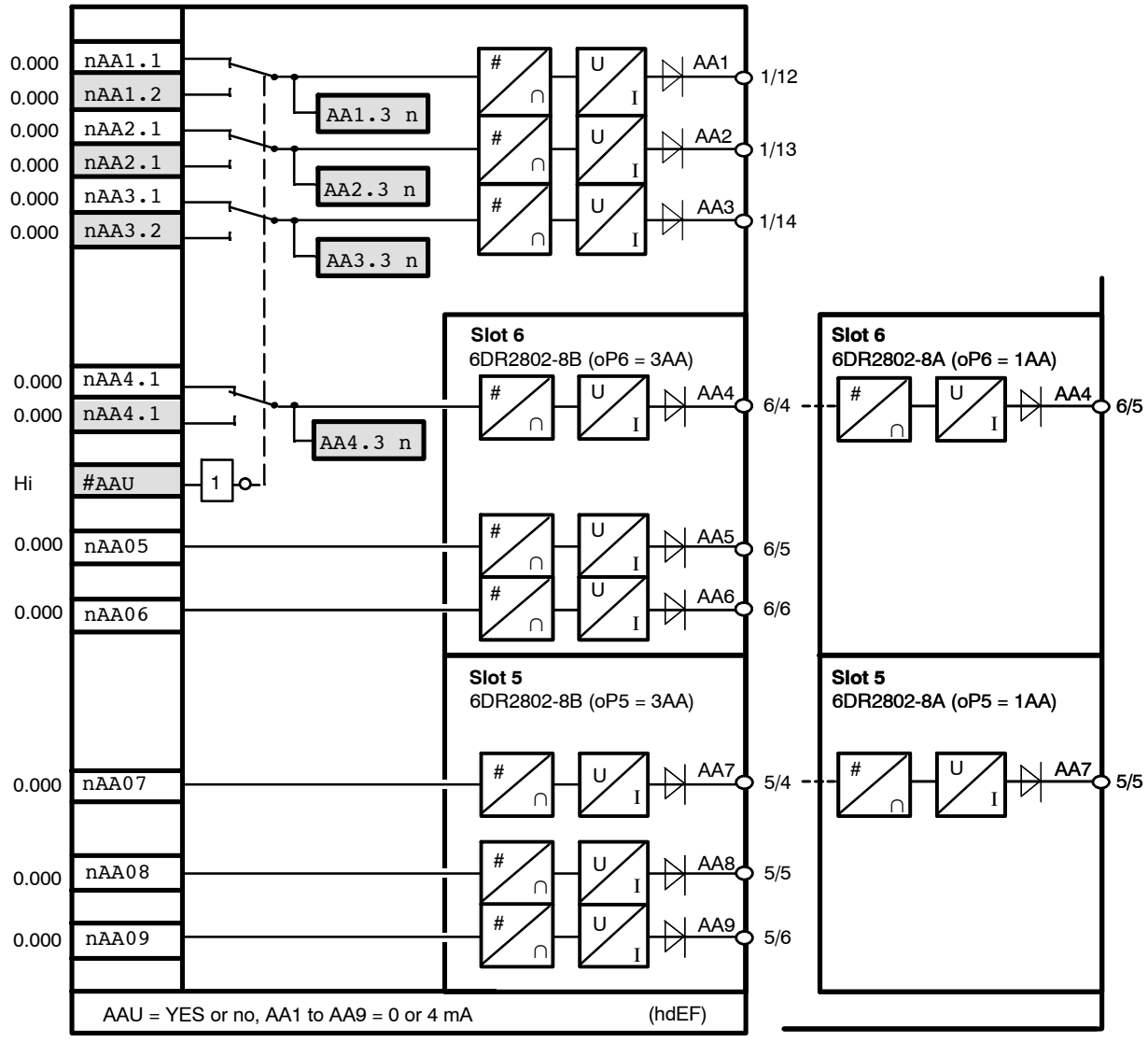
Figure 1–9 Description of the displays, keys and LEDs on the front module of the SIPART DR24

1.5.3 Output Functions

The following output functions are described in this chapter:

Analog outputs	AA1 to AA
Digital outputs	BA1 to BA16
Digital displays	dd1 to dd3 (7-segment displays)
Analog displays	dA1, dA2 (bar graphs)
LEDs	L1 to L13, L14

Analog outputs AA1 to AA9



are hidden in FCon, if AAU = no in hdEF

Figure 1–10 Output function analog outputs AA1 to AA9

- The analog outputs AA1 to AA3 are available in the standard controller.
- All data sinks AA** are defaulted with 0.000 so that the analog outputs have the value 0 (0 mA/4 mA) without further wiring.
- The analog outputs AA1 to AA3 can be wired on two channels (AA*.1, AA*.2). The data source AA*.3 allows the effective output value to be processed.
- The data sinks can be switched commonly for the four D/A converters by the control signal AAU.
- By connecting the data source AA*.3 with the corresponding data sink AA*.2, the last active value through AA*.1 can be kept constant after switching over.
- If = no is assigned to the AAU function in the configure mode hdEF, the shaded data sources and sinks do not appear in the configuring mode FCon. Since AAU is defaulted with high, the drawn switch position is then active.
- The data sinks AA*.1 and with them the analog outputs are held at the last value during configuring. If this is not desired you can switch to the data sinks AA*.2 by wiring AAU with the fault message nStr (no configuring) which can be wired for example with safety values. These values are then retained during the entire configuring process.

Digital outputs BA1 to BA16

The 16 digital outputs are distributed on the basic board and 2 slots to every 4 digital outputs (see figure 1–11, page 31). Either the signal converters for 2 relay outputs (6DR2801-8D) or for 4 voltage outputs 24 V (6DR2801-8E) can be plugged at every slot. For the relay outputs the relay contacts are output with 3 poles (switching function!). The voltage outputs are fed with 24 V by the main board of the SIPART DR24.

The 2 slots can also be equipped with modules of another function, see chapter 1.5.2, page 24. The corresponding digital outputs are then omitted.

All data sinks bA* are defaulted with low so that the digital outputs are low without further switching. The digital outputs BA1 to BA4 can be switched on two channels. The data sources bA1.3 to bA4.3 allow the effective status to be stored. In this way the data sinks for the 4 digital outputs can be switched over commonly with the control signal bAU. The last status can be retained after switching over by connecting the data sources bA1.3 to bA4.3 with the corresponding data sinks bA1.2 to bA4.2.

The shaded data sources and sinks do not appear in the configuring mode FCon if no is assigned to the bAU function in the configuring mode hdEF. Since bAU is defaulted with high, the drawn switch position is active.

The data sinks bA1 to bA16 are held at their last logical level before the switch over edge to the configuring during configuring. The digital outputs react accordingly[1)] If this is not desired, you can switch for bA*.1 to the data sinks bA*.2 which can be switched with safety levels for example by switching bAU with the fault message nStR (no configuring). These levels are then retained during the entire configuring process.

Note: This safety switching only applies for bA1 to bA4. For bA05 to bA16, it **cannot** be simulated with the fault message nstr by using digital switches because no more blocks are processed after the switch over edge to the configuring!

1) If the digital output sources are buttons (tA1.1, tA1.2, tA2.1, tA2.2 etc.), the digital outputs are set to ”low” on leaving the process level because otherwise the buttons would be ”frozen”.

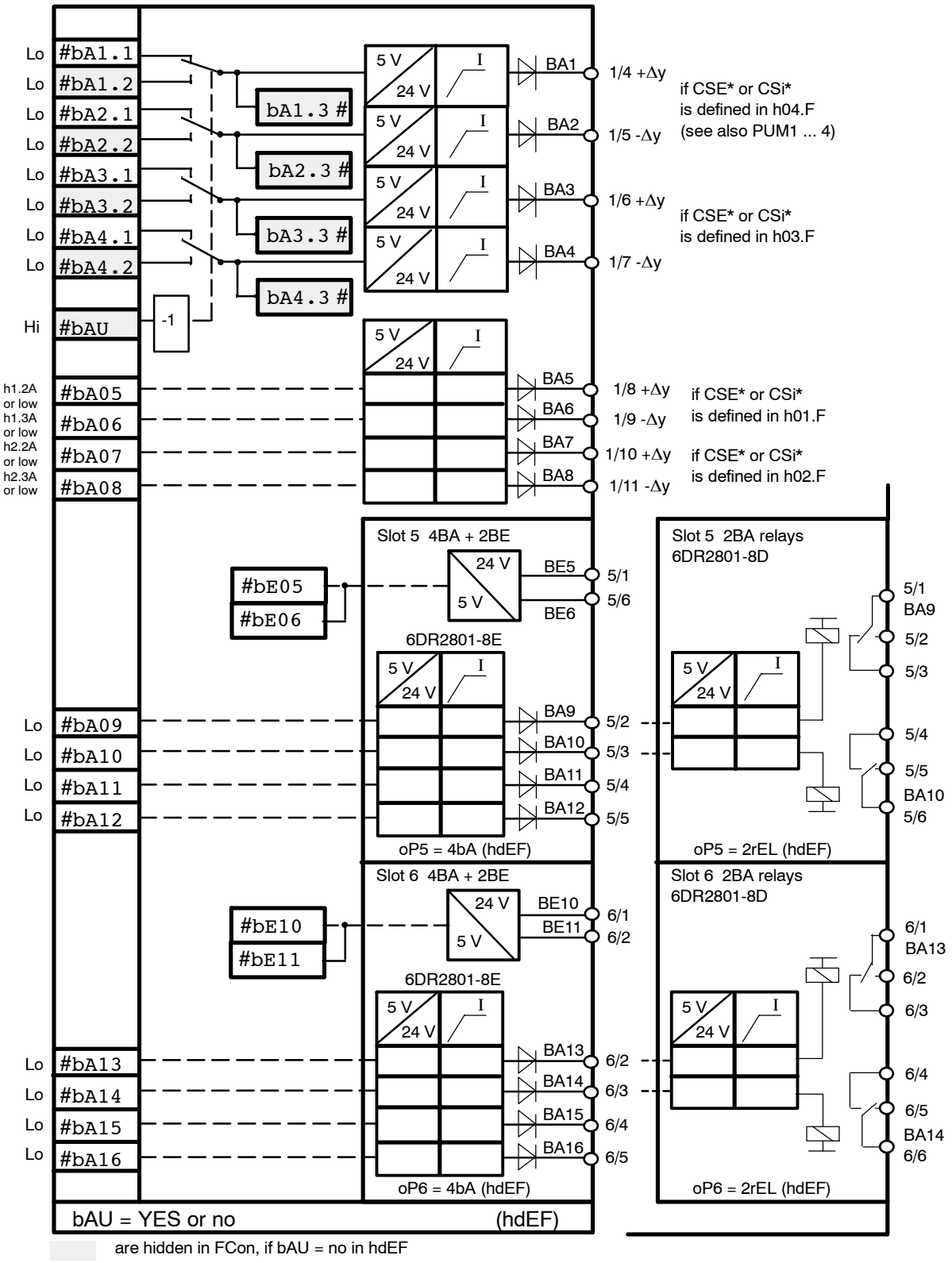


Figure 1–11 Output function digital outputs

Digital displays dd1 to dd3 (7-segment displays)

The displays serve to display the analog variables (arrangement of displays see figure 1–15, page 34). The displays can be switched between the data sinks dd*.1 to dd*.4 by the control inputs dd*.U/dd*.M for quadruple applications.
If the displays are not wired in the configuring mode FCon, the drawn switch positions become active by defaulting dd*.U/dd*.M with low and the displays go dark by defaulting dd*.1 with ncon.

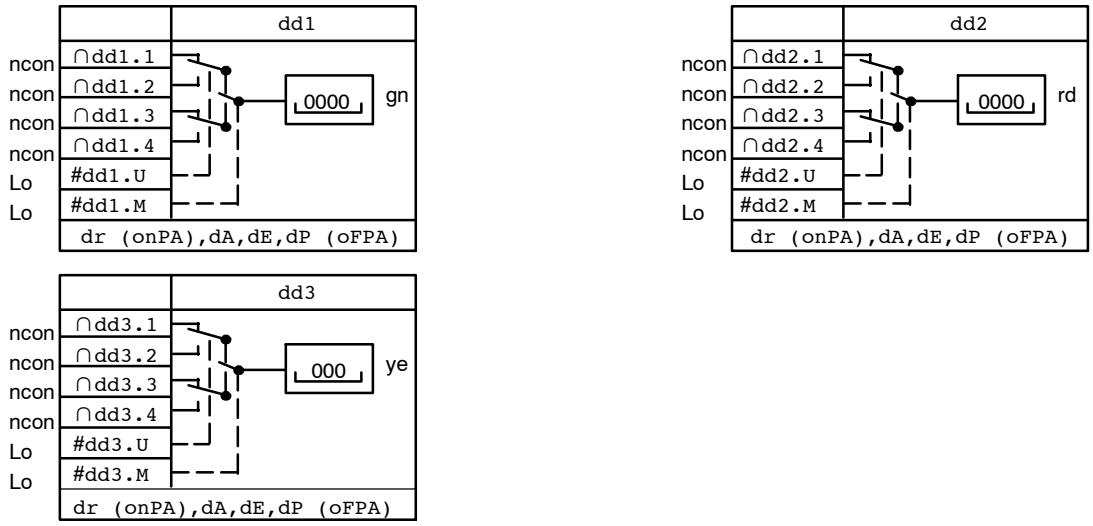


Figure 1–12 Output function digital displays

The displays have the parameters repetition rate dr (onPA), decimal point dP, start of scale dA and full scale dE (oFPA). The display comes to rest with dr for restless process variables. The display is then not activated for every cycle but for every cycle set with dr. The display is activated independently of dr in every cycle when switching between data sinks.

Start of scale dA and full scale dE specify the numeric range of the calculating value 0 to 1 or 0 to 100 % for the variable to be displayed. (Range –1999 to 19999 for dd1 and dd2, –199 to 999 for dd3). If the start of scale dA is set greater than the full scale dE, this gives a falling display with a rising input variable.

Exceeding or dropping below the operating range are displayed with oFL or -oFL ($\overline{o}$FL).

Analog displays dA1, dA2 (bar graphs)

The displays serve to display analog variables. You can switch between the data sinks dA*.1 to dA*.4 with the control inputs dA*.U/dA*.M for quadruple applications.

If the displays dA*.* are not wired in the configuring mode FCon, the drawn switch positions become active by defaulting dA*.U/dA*.M with low and the displays go dark by defaulting da*.1 with ncon.

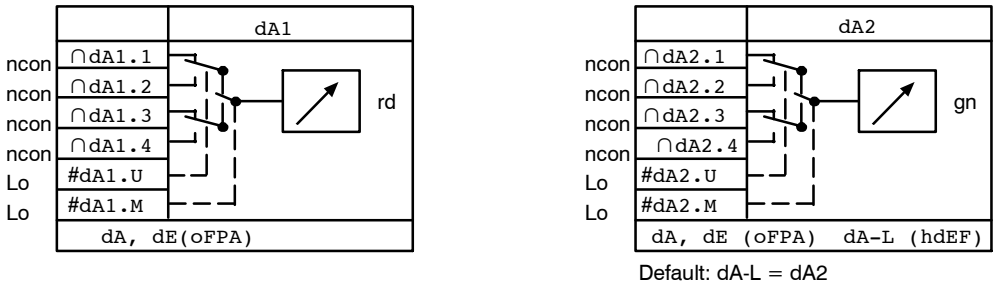


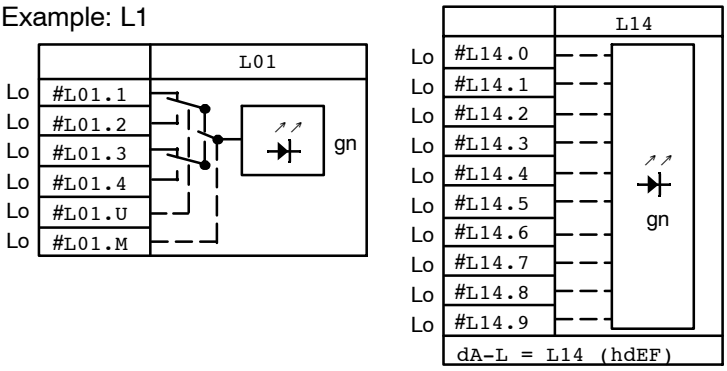
Figure 1–13 Output function analog displays

The display dA2 can also be used optionally as a LED array for analog display or status messages of 10 digital signals (L14.0 to L14.9). To do this dA–L is defined with 14 in the configuring mode hdEF. The displays dA1, dA2 have the parameters start of scale dA and full scale dE (oFPA).
The start of scale and full scale specify the numeric range of the calculating value 0 to 1 or 0 to 100 % for the displaying variable. (Range –199.9 to 199.9). If the start of scale dA is set greater than the full scale dE, this gives a falling display with a rising input variable. Start of scale 0 means that the 1st lower bar lights, at 100 % the last top bar. The other bars are evenly distributed over 100 %. Exceeding or dropping below the operating range is displayed by flashing 1st or last LED.

LEDs L1 to L13, L14

The LEDs signal digital switching states. LEDs L1 to L13 can be switched to other sources for quadruple applications with the control input L*.U/L*.M.

The drawn switch position becomes active due to defaulting with low; if the LEDs in FCon are not switched, they are dark. The LEDs L14.0 to L14.9 (bargraph bars) can be used as single diodes as an alternative to display dA2. To do this dA–L = 14 must be set in the configuring mode ndEF. The inputs are available for switching to FCon as a result.



Color	LEDs
green	L1, 2, 10, 11, 14
yellow	L3, 8, 9, 12, 13
red	L4, 5, 6, 7

Figure 1–14 Output function LEDs

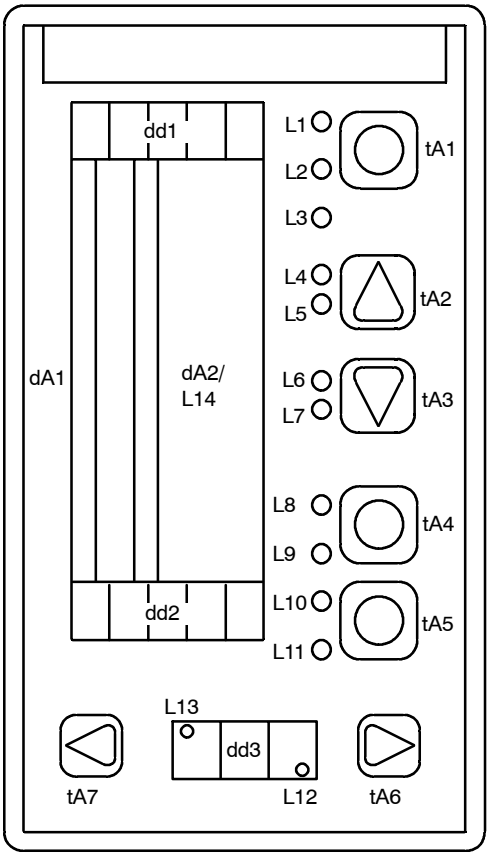


Figure 1–15 Designation of the displays, keys and LEDs on the front module of the SIPART DR24

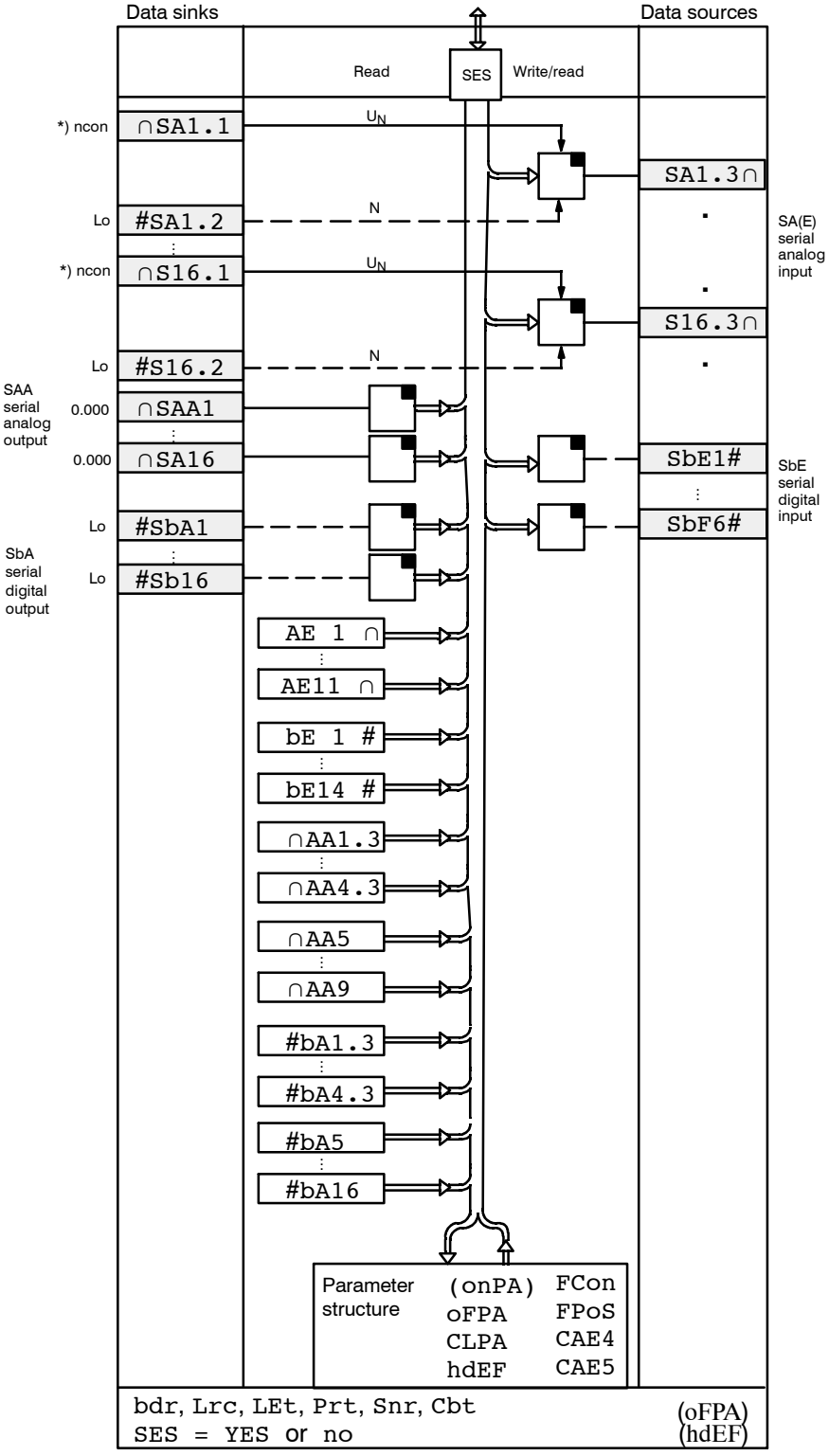
1.5.4 Serial Interface (SES) and PROFIBUS DP (Input/Output Functions)

The input and output (write and read) of the SES includes freely switchable inputs and outputs (SAE, SbE or SAA, SbA) and permanently assigned read only inputs and outputs (AE, BE or AA, BA) of the SIPART DR24. In addition the parameters and the configuration data can be written and read. For further explanations of the interface traffic (procedure, address ranges, data format), see Instruction Manual C73000-B7476-C135 (edition ≥ 4) and type GSD file.

The data sinks SA(E)*.1 (tracking variable) and SA(E)*.2 (control signal tracking) serve to track the data source SA*.3 when switching between this data source and another source and the switching in the direction SA(E)*.3 is to be bumpless. No tracking takes place due to the defaulting of SA(E)*.2 with low.

The interface communication can be monitored for cyclic processing. A monitoring time can be defined with the private parameters Cbt; if the time interval between two telegrams is greater than the defined monitoring time, the digital input SbE1 is set to low. As a result switching processes could be triggered.

If SES data sources are connected with the sinks bLS, bLPS or bLb, they are set to low when the monitor responds or at Cbt = oFF (SES–OFPA) (see also chapter 3.3.7, table 3–8, page 157)!



*) Default: 0.000

are hidden in FCon, if SES = no in hdEF

Figure 1–16 Input/output function of the serial interface

Restart conditions:

Power on	SA1.1...SA16.3	SbE1...SbF6
bAtt = no	0.000	Lo
bAtt = YES (hdEF)	last value	last status

1.5.5 Data Sources with Message Function (Digital Outputs #)

General messages

tACt#

Clock output
This output generates one clock signal in 1:1 rhythm with a period of approx. 1 s. The data source is available for free switching in Fcon.

tAC1#

Clock signal
with parameterizable (in controller cycles)
period (onPA : tAC1 / PEr)
and turn–on time (onPA : tAC1 / tAS)

tAC2#

Clock signal with parameterizable (in controller cycles)
period (onPA : tAC2/ PEr)
and turn–on time (onPA : tAC2/ tAS)

rES1#

Reset signal
serves to reset blocks with memory function;
High in the first cycle (after restarting the controller), then Low.

rES#

Reset signal
serves to reset blocks with memory function;
High in the first and second cycle (after restarting the controller), then Low.

AdAP#

This output provides information about the status of the adaptation procedure (see also chapter 3.3.2, page 138).

Low: Before adaptation after aborting adaptation or after exiting adaptation when mode tA1 is left
High/low clock: during adaptation
High: end of adaptation before leaving the adaptation mode

Fault messages

The SIPART DR24 provides a number of fault messages for switching and evaluating:

AE1↳ to AE11↳ # , **nAE↳ #**

The analog inputs AE1 to AE11 are monitored for exceeding or dropping below the limits of the range of 3 % and +103 %. For the individual input the AE* ↳ signal is available (high: exceeding limit) * = 1 to 11.

The negated and or-linked group message is offered with the data source nAE ↳.

nAE↳ = $\overline{\text{AE}\downarrow}$ (High: no exceeding of limit)

AE↳ = AE1↳ VAE2↳ V to V AE11↳

nPon#

High: no power on reset

Every power on triggers a reset for the CPU and sets nPon to low. An optical signaling by flashing of displays dd1 to dd3 when restarting can be configured with hdEF (dPon = YES). The flashing and nPon can be acknowledged by the key tA5 (first press after power on or manual reset) or by alarm polling with the SES.

nPar#

High: no parameterization

The signal is low when the parameterization preselection mode, the onPA mode or the AdAP mode is selected. This can be done manually on the front panel or through the SES.

By switching this source with switches, the displays not used in the PAr level can be switched to other variables for example.

nStr#

High: no configuring

The signal is low in the parameterization preselection level and the different configuring modes. The configuring modes are reached manually through the front, the SES or error messages (see chapter 1.5.6, page 38). If the output reactions are to be varied in the configuring modes, the nStr signal can trigger the switchings with the appropriate switches (Aso, bSo).

oPEr#

Sum message option card error

1.5.6 Error Messages

The SIPART DR24 runs numerous error search routines automatically and reports the errors on the displays dd1, dd2. This assumes that the function is only disturbed to the extent that the error messages can still be output. If several errors occur simultaneously, the first detected error is displayed according to the processing priority. Every error elimination leads to a new error check with the appropriate reactions so that the next error then runs up. Some errors can be acknowledged or corrected, whereby it is useful to correct the errors. Some of the errors can also be corrected through the SES.

Distinctions are made between the following groups of error messages:

- Error messages when configuring the SIPART DR24, memory error
- Notes on the error messages
- Error messages for the display area of the display
- Error messages of the adaptation
- Error messages of the CPU with respect to important hardware components as well as the data communication with the controller periphery

Every group is divided into several error messages which are combined as follows.

Error messages when configuring the SIPART DR24, memory error
(see also chapter 3.3.6, page 152 (configuring mode FdEF), 3.3.7, page 155 (configuring mode FCon), 3.3.8, page 159 (configuring mode FPoS))

Some of the errors should be eliminated otherwise the programs cannot run. The other “errors” are acknowledgeable and you can switch to online mode. By acknowledging, the part of the program configured up till now can be stored in the non–volatile EEPROM (user memory).

dd1 dd2	Meaning	Version	Effect	Remedy
APSt MEM [1]	User program memory has the factory setting	If the configuring mode is exited manually or after power on	Device without concrete function; nStr = Low	Go to the parameterization or configuring mode (see chapter 3.3.1, page 136 or 3.3, page 135) and change there
FdEF Err1 [2]	Illegal function ID	If configuring mode is left manually or through SES or after power on	Configuring mode is retained or the configuring mode is switched to; nStr = Low	Automatic operation, signaled by LEDs
FdEF Err2 [2]	Illegal multiple definition of a complex function			Press the Enter key, respective erroneous position in the configuring mode appears. Correction by adjustment keys ▲, ▼, then Exit key until process mode; nStr = high
hdEF Err [2]	Illegal configuring switch contents			
FCon Err [2]	Illegal connection of source and sink			
FPoS Err1 [2]	Illegal positioning address			
FPoS Err2 [2]	Illegal multiple positioning of a function block			
FPoS Err3 [2]	Illegal positioning of an undefined function block			
ncon Err [2], [3]	There are data sinks in FCon which have not yet been switched			Press the Enter key: first ncon data sink appears or press Exit key; Exit LED off, nStr = high. Error is acknowledged, switching to online operation takes place
Item Err [2], [3]	Defined blocks or complex functions are not positioned	If configuring mode is left manually or through SES or after power on	Configuring mode is retained; nStr = Low Exit LED flashes	Press the Enter key: first nPos number appears, pay attention to correct position! or press Exit key: Exit LED off, nStr = high. Error is acknowledged, switching to online operation takes place
nPoS Err [2], [4]	Non–positioned number within a positioning row			Press the Enter key: first nPos number appears or press Exit key: Exit LED off, nStr = high. Error is acknowledged, switching to online operation takes place

1) If no control element has been assigned to the front after changing the factory setting, the front remains totally dark in online!
2) Errors can also be eliminated through the serial interface (SES).
The correction possibilities through the SES can be found in the SES description C73000-B7400-C135 (Edition ≥ 4)
3) Programs should be completed (see following instructions).
4) program only runs to positioning gap after acknowledgement.

These errors do not occur in front panel operation. In the case of data specifications through the SES in the configuring range it is very easy to make errors which can be avoided in this way.

Table 1-1 Error messages (in diminishing order of priority)

Notes on the error messages

- **ncon Err**
  It is also permissible to terminate the wiring with data sinks identified by ncon. However, it is advisable to add the missing connections because the desired functions cannot run with undefined inputs.

  If the configuring preselection level is exited by the Exit key (tA1), the flashing error message ncon Err appears if data sinks (inputs) are still marked ncon. The configuring preselection level is not exited, the error should be corrected.

  Corrections:
  The error is acknowledged by pressing the Enter key (tA4). It returns to the configuring mode FCon to the first data sink marked ncon, the error can be corrected.

  Cancel:
  If you want to cancel the connection prematurely, press the Exit key (tA1) again after the error message so that the online mode is switched to. The previous switchings are then saved in a non–volatile memory.

- **–PoS Err**
  Ending positioning with non–positioned (but defined) functions is allowed. If the configuring preselection level is to be exited with the Exit key, the flashing error message –Pos Err appears for non–positioned functions. The configuring preselection level is not exited, the error can be corrected.
  The error message is acknowledged by pressing the Enter key. It jumps back to the configuring mode FPos to the first positioning number marked by nPos. The error can be corrected or the online mode can be switched to by pressing the Exit key.

- **nPoS Err**
  Ending positioning with a positioning row with nPos gaps is allowed.
  If the configuring preselection level is to be exited with the Exit key and nPos gaps still exist, the flashing error message nPos Err appears. The configuring preselection level is not exited, the error can be corrected. The error message is acknowledged by pressing the Enter key. It jumps back to the configuring mode FPos to the first positioning number marked by nPos. The error can be corrected or the online mode can be switched to by pressing the Exit key.

Error messages for the display area of the displays dd1, dd2, dd3, dA1, dA2

oFL	Exceeding the display range (19999 or 999) of the displays dd1, dd2 or dd3
–oFL, (oFL)	Dropping below the display range (–1999 or –199) of the displays dd1, dd2 or dd3

Flashing 1st or last LED of the analog display dA1, dA2: dropping below or exceeding the display range.

Error messages of the adaptation

see chapter 3.3.2, Table 3-2, page 143

Error messages of the CPU

Error Message dd1 dd2	Monitoring of	Monitoring time	Reactions							Primary cause of error/ Remedy
			y_{hold} module			Standard controller		Options [2]		
			$\overline{St}$	AA4 with U_H	AA4 without U_H	AA1 to 3	BA1 to 8	BA9 to 12	BA13 to 16	
CPU Err	EEPROM, RAM, EPROM	Power on reset	0	last value	0 mA	0 mA	0	0	0	Monitored components of the CPU defective/ change main board
		Watch dog reset			last value					
MEM Err	User program memory	Power on reset	0	last value	0 mA	0 mA	0	0	0	User program memory not plugged or defective/plug or change
		Watch dog reset			last value					
		when storing		continues operating with current data				continues operating with current data		
oP.5.*.[1]	Data communication µP slot 5	cyclic	0					last state or undefined	continues operating with current data	Option not plugged, defective or setting in hdEF does not correspond to the plugged option/plug in option or exchange or correct oP5 [3]
oP.*.6.[1]	Data communication µP slot 6	cyclic	0	pulled last value	pulled 0 mA	continues operating with current data		operates with current data	last state or undefined	Option not plugged, defective or setting in hdEF oP6 does not correspond to the plugged option/plug in option or exchange or correct oP6 [3]
				defective, undefined						

[1] Double error display oP.5.6 also possible, * means digit dark.
[2] At BE5 to 9 and BE10 to 14 the effect of the digital inputs (after inversion) are set to 0 in the event of an error.
[3] IF oP5/oP6 2BA relay is selected, there is no monitoring.

Table 1-2 Error messages of the CPU

1.5.7 Basic Functions (Arithmetic blocks b)

1.5.7.1 General

In the SIPART DR24 a library of basic functions is stored (see figure 1–18, page 42). These basic functions can be assigned in any order to the (initially empty) 109 arithmetic blocks (see configuring mode FdEF, chapter 3.3.6, page 152). Every basic function is marked by a short name which appears in the FdEF cycle on dd1.

Every arithmetic block b**.F (** corresponds to 01–h9) has up to 3 inputs (data sinks) E1, E2, E3 and one output (data source) A. Depending on the kind of function, the input and output variables are digital (identification #, dotted lines) or analog (identification ∩, continuous lines).

The unassigned inputs (data sinks) of the functions (ncon: not connected) must be linked with data sources in the configuring mode FCon. Some data sinks are defaulted with values or logical signals (Hi, Lo), which correspond to frequent applications. These inputs can be overwritten in the FCon mode or their defaulting retained.

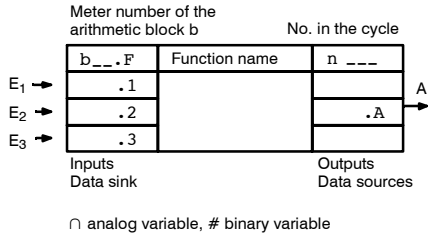


Figure 1–17 Format of an arithmetic block

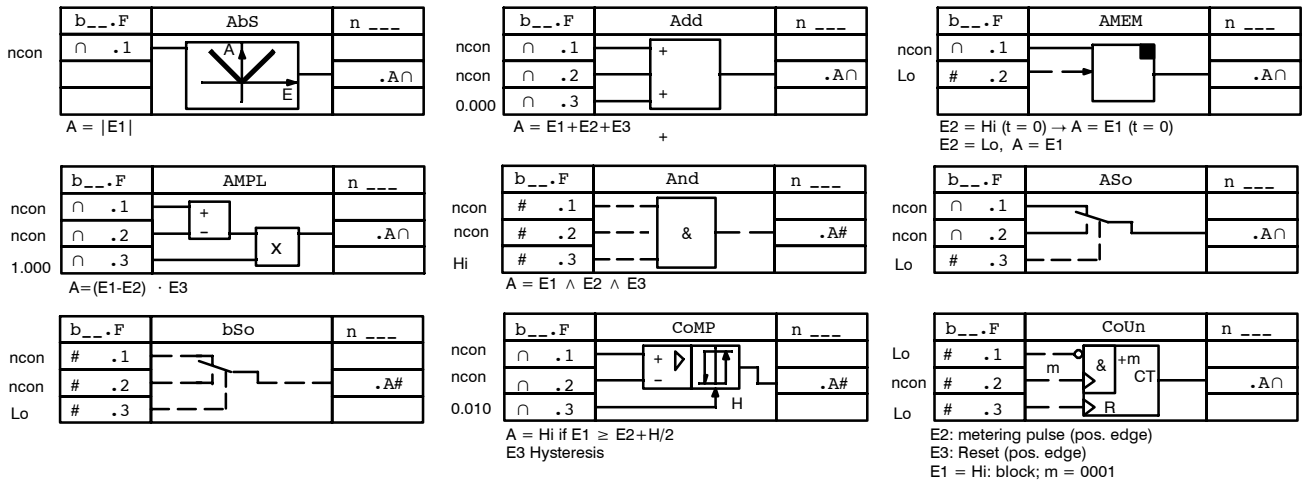


Figure 1–18 Basic functions of the SIPART DR24

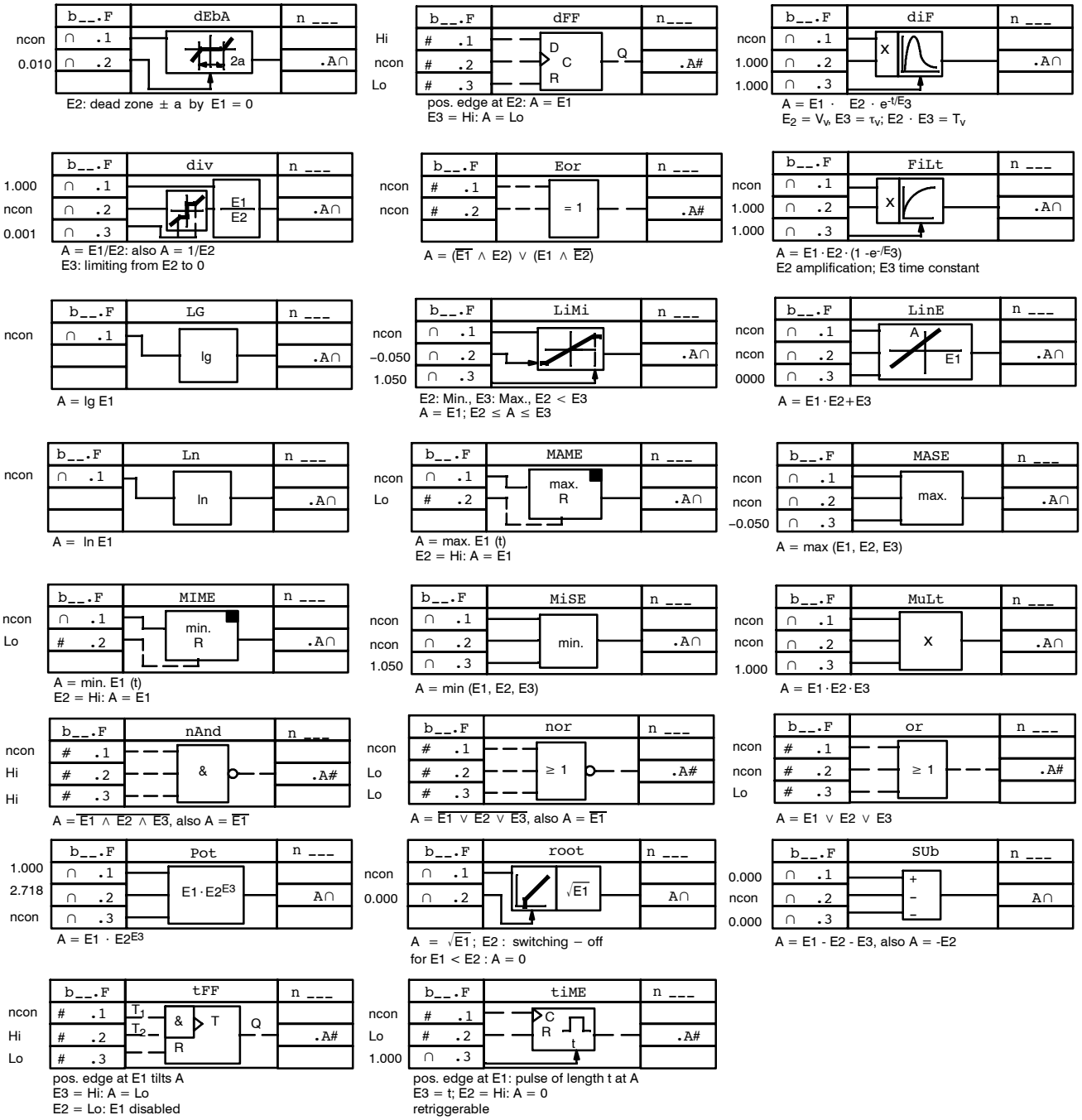
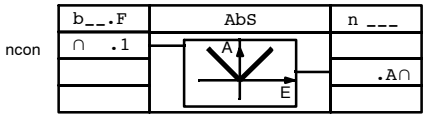


Figure 1−18 Basic function of the SIPART DR24 (continued)

1.5.7.2 Mathematical Functions

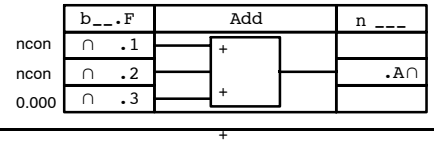
Absolute value

A = | E1 |



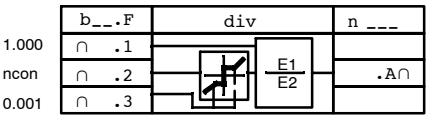
Adder

A = E1 + E2 + E3
with default: A = E1 + E2



Divider

A = E1/E2
with default: A = 1/E2



Definitions:

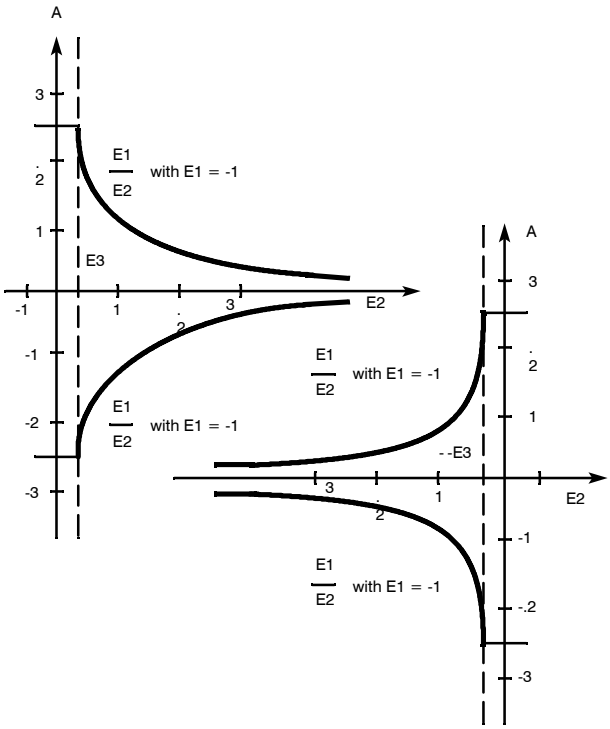
0/number = 0, 0/0 = 0,
$\pm$number/0 = $\pm 10^{19}$

E2 can be limited by E3. This prevents the output jumping between $+10^{19}$ and -10^{19} at lower values of E2 (about ± 0) and becomes very restless due to the great steepness. If you do not want this limit, E3 must be assigned 0.000.

E3 $>$ 0
Minimum value limiting of E2 to the value of E3 (division only in the 1st and 4th quadrants).

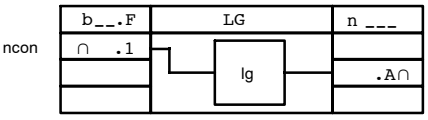
E3 $<$ 0
Maximum evaluation of E2 to the value of E3 (division only in the 2nd and 3rd quadrants).

E3 = 0
No limiting of E2 (division in all 4 quadrants with pole position at E2 = 0).



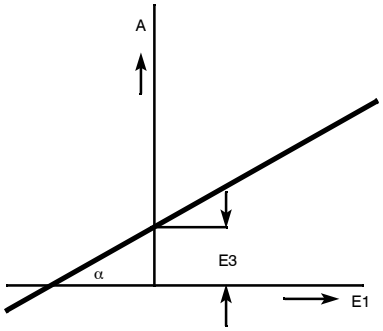
Decadic logarithmer

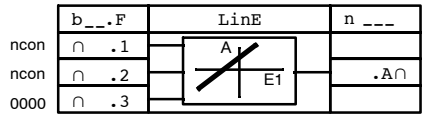
A = lg E1 E1 $>$ 0
E1 $\leq$ 0, A = -10^{19}



Linear equation

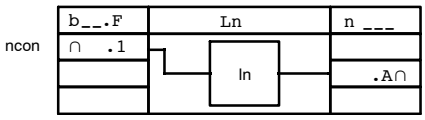
A = E1 · E2 + E3
tanα = E2 = A/E1
Default A = E1 · E2





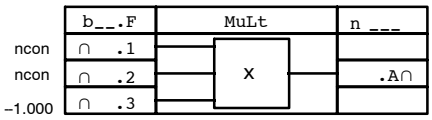
Natural logarithmer

A = ln E1 E1 > 0
E1 ≤ 0, A = -10^{19}



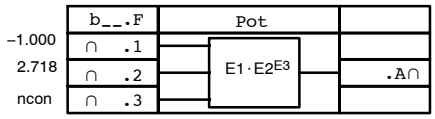
Multiplier

A = E1 · E2 · E3; with default: A = E1 · E2



Exponential function

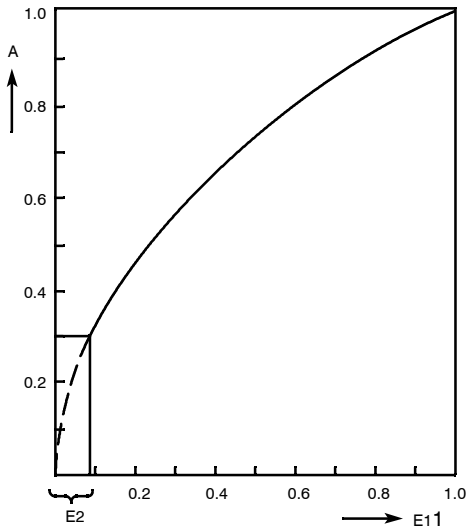
A = E1 · $E2^{E3}$
A = e^{E3} (default)

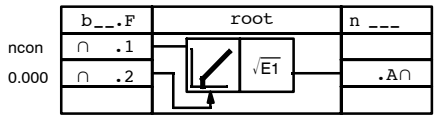


Rooter

A = $^{2}\sqrt{E1}$

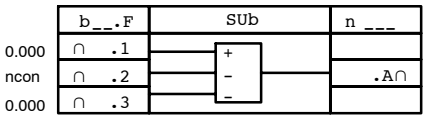
The equation only applies for positive E1, negative E1 are set equal to zero. The output can be set to zero with E2 for lower values of E1, i.e.
A = 0 for E1 ≤ E2





Subtractor

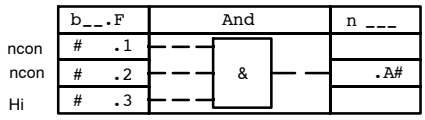
A = E1 – E2 – E3; with default: A = –E2
With the default, this function acts as a negation for E2



1.5.7.3 Logical Functions

AND function (AND)

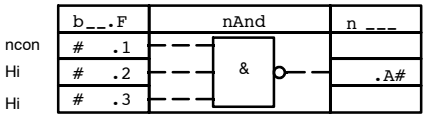
$A = E1 \wedge E2 \wedge E3 = \overline{\overline{E1} \vee \overline{E2} \vee \overline{E3}}$
with default: $A = E1 \wedge E2$



E1	E2	E3	A
0	0	0	0
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	1

NAND function

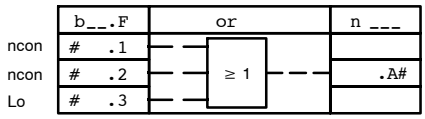
$A = \overline{E1 \wedge E2 \wedge E3} = \overline{E1} \vee \overline{E2} \vee \overline{E3}$
with default: A = E1 (Negation of E1)



E1	E2	E3	A
0	0	0	1
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	0

OR function

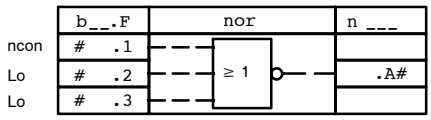
$A = E1 \vee E2 \vee E3 = \overline{\overline{E1} \wedge \overline{E2} \wedge \overline{E3}}$



E1	E2	E3	A
0	0	0	0
1	0	0	1
0	1	0	1
1	1	0	1
0	0	1	1
1	0	1	1
0	1	1	1
1	1	1	1

NOR function

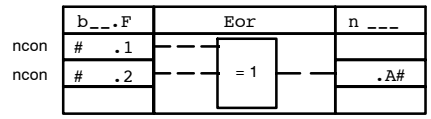
$A = \overline{E1 \vee E2 \vee E3} = \overline{E1} \wedge \overline{E2} \wedge \overline{E3}$
with default: $A = \overline{E1}$ (Negation of E1)



E1	E2	E3	A
0	0	0	1
1	0	0	0
0	1	0	0
1	1	0	0
0	0	1	0
1	0	1	0
0	1	1	0
1	1	1	0

Exclusive OR function (EXOR)

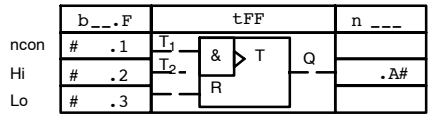
$A = (\overline{E1} \wedge E2) \vee (E1 \wedge \overline{E2}) = \overline{(E1 \vee \overline{E2}) \wedge (\overline{E1} \vee E2)}$



E1	E2	A
0	0	0
1	0	1
0	1	1
1	1	0

T–flip–flop

Every positive edge at T = E1 ∧ E2 (toggle) flips the output to the respective other position. High at E3 (Reset) sets A to low and blocks E1 and E2.



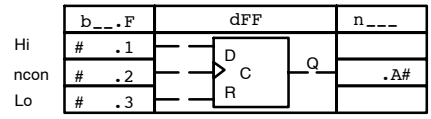
E1 (T1)	E1 (T2)	E3 (R)	A (Q)	Remarks
x	x	1	0	
	1	0	Qo → $\overline{Qo}$	Q flips to the other position
1	↗	0	Qo → $\overline{Qo}$	
0	x	0	Qo	saved
x	0	0	Qo	

Restart conditions after power failure:

Power on	Output A
bAtt = no	0
bAtt = YES (hdEF)	last status

D–flip–flop

Every positive edge at E2 (C = Clock) sets A to E1 (D = file). Hi at E3 (R = Reset) sets A to low and blocks E2.



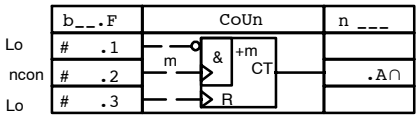
E1 (D)	E2 (C)	E3 (R)	A (Q)	Remarks
x	x	1	0	
1	↑	0	1	
0	↑	0	0	
x	0/1	0	Qo	saved

If shift registers are switched with the D–flip–flop, the positioning must be reversed due to the serial processing, i.e. the first stage is processed last.

Restart conditions after power failure:

Power on	Output A
bAtt = no	0
bAtt = YES (hdEF)	last status

Counter



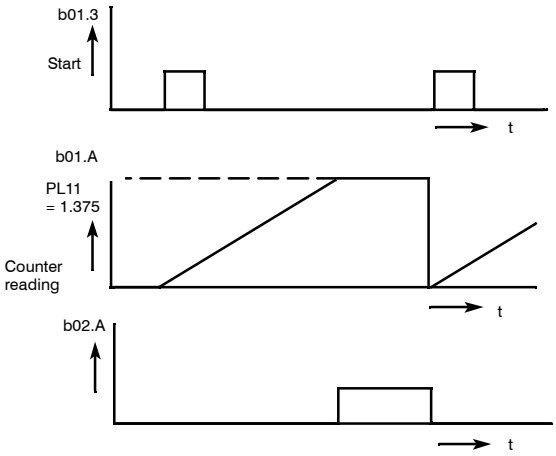
Every positive edge at E2 (m) counts A 0.001 upwards when E1 = low. Every positive edge at E3 (Reset) sets A to 0.000. The counting range goes up to 50000 · 0.001 = 50; other counting pulses are not evaluated. If the output of the counter is switched with the displays dd1 or dd2 (dA = 0, dE = 1000, dP = ⊟⊟⊟⊟)a maximum of 10000 counting pulses can be displayed, then oFL appears. Only one counting pulse per 2 computing cycles can be evaluated. If a control signal is to be output dependent on the counter reading, the basic function Comparator (CoMP) must be connected with the counter and the counter reading compared with an adjustable parameter (PL**) (see figure 1–19 and 1–20, page 48).

E1	E2 (m)	E3 (R)	A	Remarks
x	x	↑	CT = 0.000	Reset
1	x	1/0	CTo	1)
0	↑	1/0	CT+n · m	Counting process

1) Counter reading saved, count input blocked

Restart conditions:

Power on	output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value



Example:
1375 = 1.375/0.001 pulses are to be counted from the start. The counter reading is shown on one display and is retained until a new start command.

Figure 1–19 Dependence of the output signals on the input signals at the counter

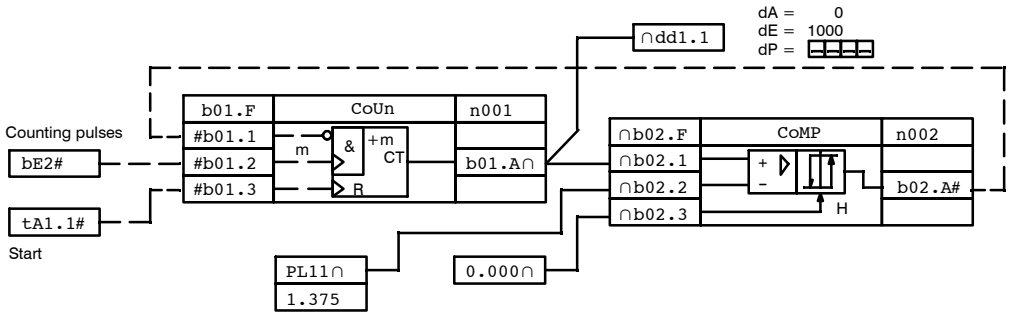
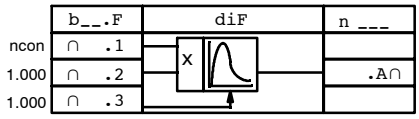


Figure 1–20 Connection of a counter with a comparator; at the specified numeric value 1.375 (corresponds to 1375 metering pulses) a high signal is output by CoMP

1.5.7.4 Timing Functions

Differentiator (high pass)



A = E1 · E2 · $e^{-t/E3}$
With E2 (V_v) = derivative gain
E3 (T_v) = derivative action time constant [s]

Use for control technical applications:
$T_v = V_v \cdot \tau_v$ = derivative action time

Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value

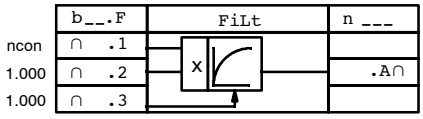
Example curve calculation:

with E2 = const. and $\frac{\Delta E1}{\Delta t}$ = const.

$$A = E2 \cdot E3 \cdot \frac{\Delta E1}{\Delta t}$$

Recommendation : $E3 \ll \frac{\Delta E1}{\Delta t}$
(approx. 0.01)

Filter (low pass)

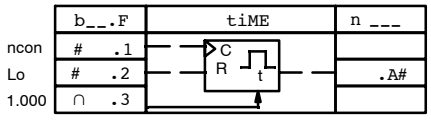


A = E1 · E2 $(1 - e^{-t/E3})$
With E2 = gain
E3 = time constant [s]
Default: A = E1 $(1 - e^{-t})$

Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value

Timer (monoflop)



Every positive edge at E1 (C) outputs a pulse with length t = E3 at A. While A = high another positive edge at E1 can output a pulse with length t again (re-trigger). High at E2 (Reset) sets A to low and blocks E1. Values at E3 for the pulse length in seconds are limited to 1 to 7500.

E1 (C)	E2 (R)	Output A
x	1	0
↑	0	1 (duration t)

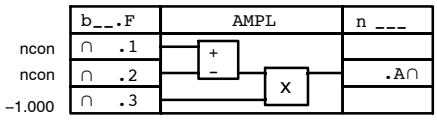
Restart conditions:

Power on	Output A
bAtt = no	0
bAtt = YES (hdEF)	last status, time continues running from turn off time

1.5.7.5 Comparison and Switching Functions

Differential amplifier

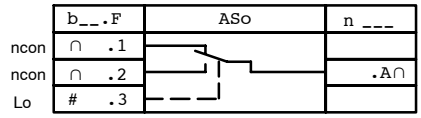
A = (E1 – E2) · E3
With E3 = gain factor
Default: A = E1 – E2



The differential amplifier is used primarily for forming the control difference xd = w – x with the possibility of active direction reversal (normal/reversing) by E3 = –1.000.

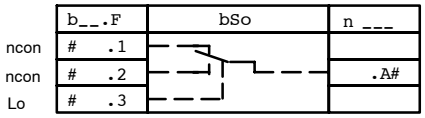
Switch for analog variables

E3	A
0	E1
1	E2



Switch for digital variables

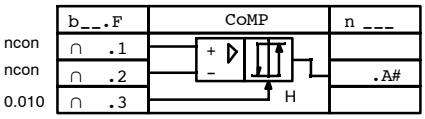
E3	A
0	E1
1	E2



Comparator with adjustable hysteresis

(two–position switch, e.g. limit value sensor)

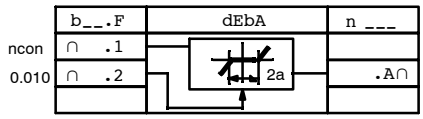
Inputs	Output A
E1 ≥ (E2 + H/2)	1 (H = |E3| = hysteresis)
E1 < (E2 – H/2)	0



If the input variables are formed by computing, the comparator may respond shifted by 1 LSB due to the computing error.

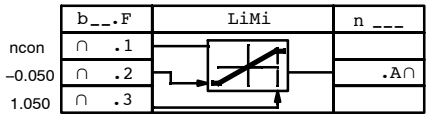
Response threshold (dead band)

A = 0 for |E1| ≤ |a|,
A = signum E1 · (|E1| – |E2|) for |E1| > |a|
with a = 32 = response threshold



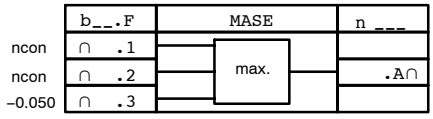
Limiter

The signal at E1 is limited to the values set with E2 and E3.
E2 = lower limit
E3 = upper limit
With E2 ≥ E3 A is = E3



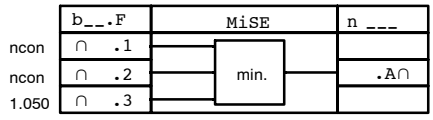
Maximum selection

The greatest of the three input values is connected through to A:
A = max. (E1, E2, E3)



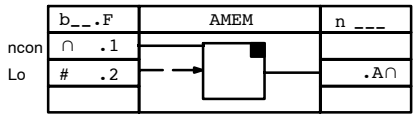
Minimum selection

The lowest of the three input values is connected through to A:
A = min. (E1, E2, E3)



Analog memory

The output is held at E2 = high at the value applied to input E1.
At E2 = low the memory is tracked to the value applied at input E1.

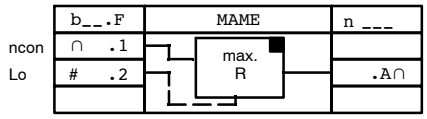


Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value

Maximum memory

The greatest value at E1 over time t is saved at E2 = low and appears at A:
A = max E1(t)
High at E2 (Reset) sets A to E1.

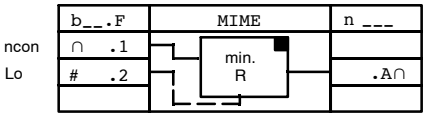


Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last max value

Minimum memory

The lowest value at E1 over time t is saved at E2 = low and appears at A:
A = min E1(t)
High at E2 (Reset) sets A to E1.



Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last min value

1.5.8 Complex Functions (Arithmetic blocks c, d, h)

1.5.8.1 General

In addition to the basic functions, the SIPART DR24 contains a number of complex function blocks (Figure 1–21, page 53). The application frequency per function type is permanently defined. The respective complex function block is assigned to specific arithmetic blocks (c, d, h) as required in the programming mode FdEF (see chapter 3.3.6, page 152) as in the basic functions. Every arithmetic block type can be assigned a different number of times (c: 33 times, d: 4 times, h: 4 times). Every function has a short name which appears in FdEF on dd1.

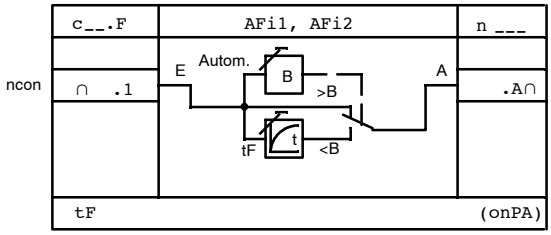
Frequently recurring problems are already realized in the complex function blocks; e.g. the PID controller. Most of these solutions are stored several times; in this way the PID controllers (blocks h) can be assigned a total of four times from the function supply of 12 functions for example: CCn1, 4 (K–controller), CSi1, 4 (S–controller with internal feedback) or CSE1,4 (S–controller external position feedback).

There is no uniform number of inputs and outputs for the complex functions. It depends on the function depth. Inputs and outputs are numbered consecutively and the outputs are identified by A if this is technically possible in the display. As in the basic functions, many inputs are defaulted with numeric values or logical status signals in the complex functions. These inputs can be overwritten in the FCon mode or their defaulting retained. The inputs which are not defaulted are identified by ncon, i.e. they must be linked with data sources in the configuring mode FCon. Inputs and outputs for analog signals are marked by ∩, inputs and outputs for digital signals are marked by #.

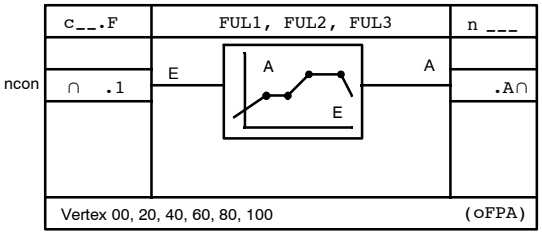
The complex functions have partly their own („private”) parameters which can be set as online or offline parameters (see chapter 3.3.1, page 136 and 3.3.3, page 145). For example, the PID controllers have the private parameters Kp, Tn and Tv among others.

1.5.8.2 Arithmetic Blocks c01.F to c33.F

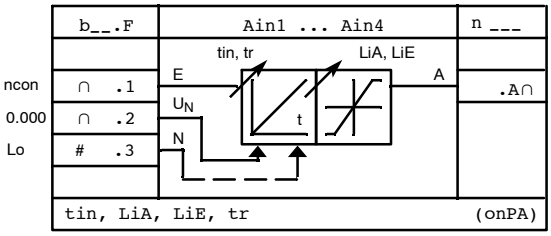
These blocks can be assigned with functions in FdEF up to 33 times. The individual functions are available 2 or 3 times (see header of the block).
The blocks have 1 to a max. 4 inputs and one output each per function type. They have private parameters in the onPA or oFPA range.



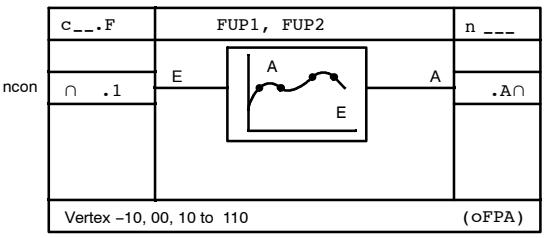
Adaptive filter AFi



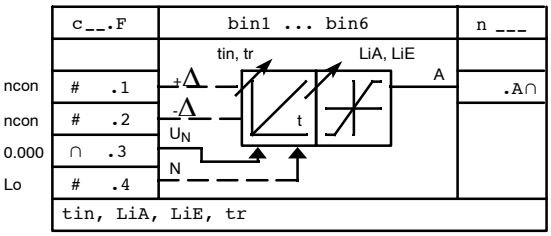
Function transmitter (linear) FUL



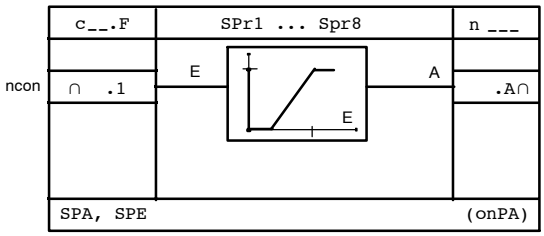
Integrator with analog input Ain



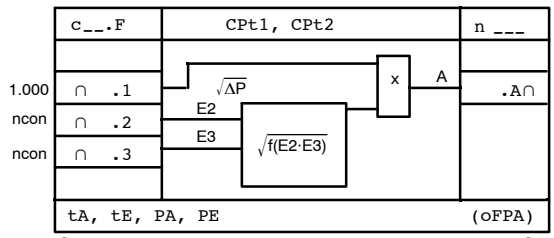
Function transmitter (parabola) FUP



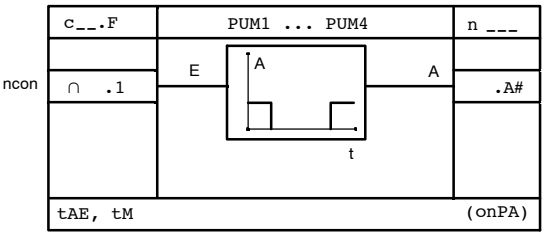
Integrator with binary input bin



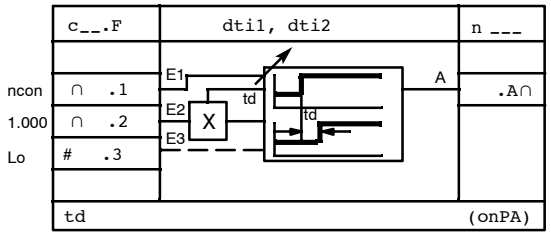
Split range SPr1 to SPr8



Correction computer pressure, temperature CPt



Pulse width modulator



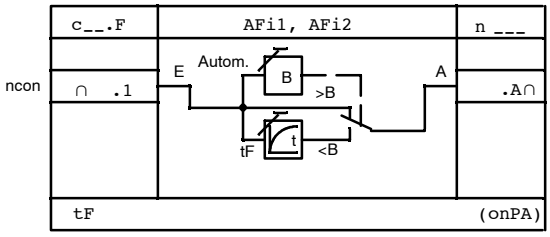
Dead time element dti

Figure 1–21 Complex functions c of the SIPART DR24

The individual complex functions are explained below in detail.

Adaptive filter AFi1, AFi2

Fault at E smaller than B : A = E(1 – e^{-t})
Fault at E greater than B: A = E



Within a band B in which periodic fault signals occur, these changes at input E (c**.1) are considered as faults by the filter and filtered with the set time constant tF. Changes in a direction leading out of the filter band are passed unfiltered to the output A (c**.A) in order to allow fast signal change in a controlled system for example. If the fault level changes in the meantime, the band automatically adapts itself to the new level (Figure 1–22).

Because the filter band sets itself automatically and B is therefore not known, the time constant tF may only be selected so great that the control loop would not oscillate even at a great filter band for control technical reasons: tF < TG (Tg = delay time of the control system). When using the D part (PD, PID) use of the adaptive non–linear filter is highly recommended because the input noise amplified by Kp · vv can be suppressed.

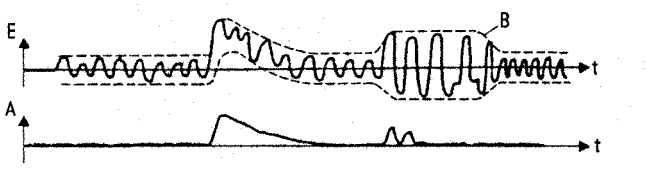
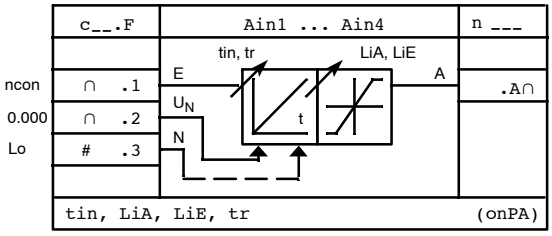


Figure 1–22 Effect of the adaptive non–linear filter

Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value

Integrator with analog input Ain1 to Ain4



$$A = \frac{1}{tin} \int_0^t E(t)dt + U_{No}$$

U_{No} = A at time t = 0
tin = 1 to 9984 s integral action time
LiA = –199.9 % to +199.9 % output limiting min
LiE = –199,9 % to +199.9 % output limiting max } LiE > LiA
tr = off,1 to 9984 s tracking time (ramp)

The integral of the variable input value E (polarity and value) is formed over the time t. The rise speed at constant E is $\tan\alpha = \Delta A/\Delta t = E/tin$.

The integrator can be tracked to the value applied at U_N (C**.2) by the control signal N = high (C**.3). The tracking time is specified by the private parameter tr.

The following applies:

$$\tan\beta = \frac{100\,\%}{t_r} = \frac{\Delta A}{T_r}$$

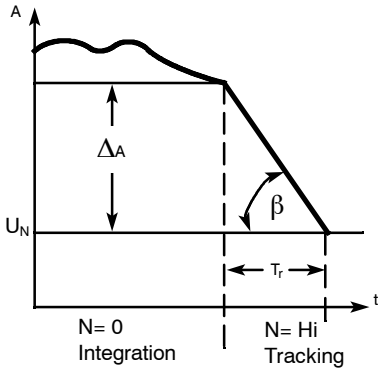


Figure 1–23 Tracking time tr

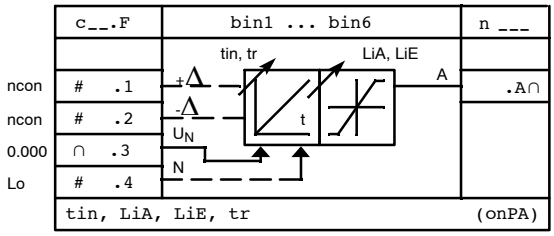
Integration and tracking are only possible within the limits set with LiA and LiE. The minimum value LiA may not be set greater than the maximum value LiE and vice versa.

At E = 0 and N = low the integrator acts as an analog memory.

Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	last value

Integrator with binary input bin1 to bin6



$$A = \frac{1}{tin} \int_0^t \pm 1 \cdot dt + U_{No};\ \pm = f(E1, E3)$$

U_{No} = A at time t = 0
tin = 1 to 9984 s integral action time, ProG
LiA = –199.9 % to +199.9 % output limiting min
LiE = –199.9 % to +199.9 % output limiting max
tr = off,1 to 9984 s tracking time

The integral of the constants ±1 (±100 %) of the control inputs +Δ (C**.1) and – Δ (C**.2) is formed dependent on the direction over the time. The rise speed is tanα = ΔA/Δt = 100 %/tin.

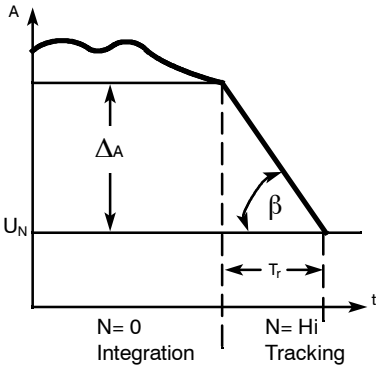
In position tin = ProG the integral speed is progressive so that setpoints set manually can be set fast and still with a high resolution when switching with the keys. The output of the integrator is saved in a non–volatile memory when bAtt = YES is set.

The integrator can be tracked to the value applied at U_N (C**.3) by the control signal N = Hi (C**.4). The tracking time is specified by the private parameter tr.

Integration and tracking are only possible within the limits set with LiA and LiE. The minimum output limit LiA cannot be set greater than the maximum output limit LiE and vice versa.

At ±Δ=Lo the integrator acts as an analog memory.

The following applies:
$\tan\beta = \frac{100\ \%}{t_r} = \frac{\Delta A}{T_r}$

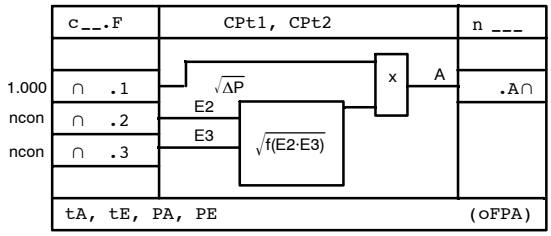


Restart conditions:

Power on	Output A
bAtt = no	0.000
bAtt = YES (hdEF)	value before turning off the power supply

Figure 1–24 Tracking time tr

Correction computer for ideal gases CPt1, CPt2



$$A = \sqrt{\Delta p} \cdot \sqrt{f\,(E2,\ E3)}$$

$$f\,(E2,\ E3) = \frac{(PE - PA)\ E2 + PA}{(tE - tA)\ E3 + tA}$$

Function block correction computer CP for ideal gases

The rooted signal of the active pressure must be applied at input c**.1. The measuring ranges are normalized to the calculation state with the parameters PA, PE, tA, tE (correction quotients start/end for pressure and temperature).

Application

The correction computer is used to calculate the flow of gases from the active pressure Δp depending on pressure and temperature. The medium must be in pure phase, i.e. no liquid separations may take place. This should be noted particularly for gases close to the saturation.

Errors due to fluctuating status variables of the medium (pressure, temperature) are corrected by the flow correction computer here.

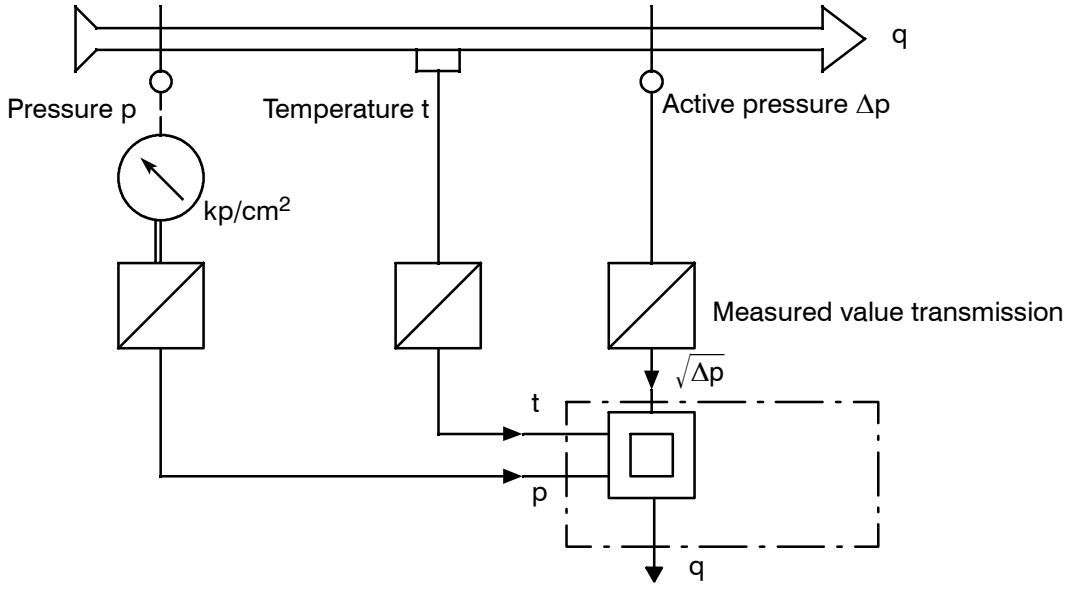


Figure 1–25 Active pressure measuring procedure, Principle

Physical notes

The active pressure measuring method is based on the law of continuity and Bernoulli's energy equation.
According to the law of continuity the flow of flowing material in a pipe is the same at all places. If the cross–section is reduced at one point, the flow speed at this point should increase. According to Bernoulli's energy equation the energy content of flowing material is made up of the sum of the kinetic energy (due to the speed) and the potential energy (of the pressure).
An increase in speed therefore causes a reduction in pressure.
This drop in pressure, the so–called "active pressure" Δp is a measure of the flow q.

The following applies: $q = c \cdot \sqrt{\Delta p}$

with c as a factor which depends on the dimensions of the pipe, the shape of the constriction, the density of the flowing medium and some other influences.
The equation states that the active pressure generated by the constriction is in the same ratio as the square of the flow.

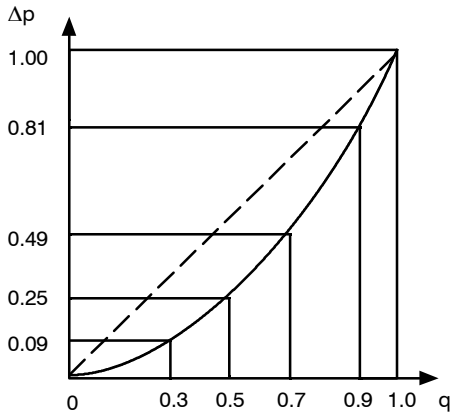


Figure 1–26 Relationship between flow q and active pressure Δp

To measure the flow, a choke is installed at the measuring point which constricts the pipe and has two connections for tapping the active pressure.
If the properties of the choke and the measuring material are known to the extent that the equation specified above can be calculated, the active pressure is a measure of the flow.

If you have chosen a certain choke, the flow can be described in the calculation state or operation state.

$q_B = K \cdot \sqrt{\varrho_B} \cdot \sqrt{\Delta p}$ or $q = K \cdot \sqrt{\varrho} \cdot \sqrt{\Delta p}$

Since the density is included in the measuring result according to the above equation, measuring errors occur when the density in the operating state differs from the value based on the calculation of the choke. Therefore a correction factor F is introduced for the density.

$$F = \sqrt{\frac{\varrho}{\varrho_B}} = \sqrt{\frac{V_B}{V}}$$

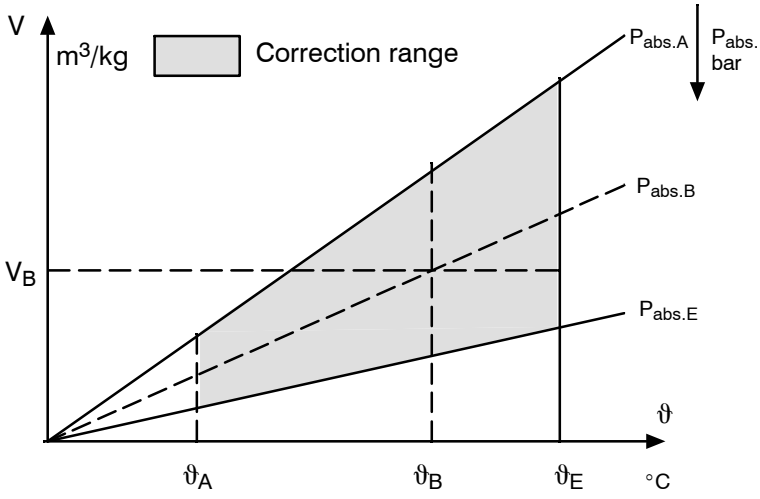
with $V = \frac{1}{\varrho}$

as specific volume.

In order to be able to perform the correction with the factor F, the current specific volume must be determined first.
For the dry gases the densities change according to the laws for ideal gases:

$$V = R\frac{T}{p} = \frac{1}{\varrho}$$ The correction factor is then given as: $$F = \sqrt{\frac{T_B \cdot p}{p_B \cdot T}}$$

with p as absolute pressure and T as absolute temperature.



$P_{abs.A}$ to $P_{abs.E}$	Range of the pressure transmitter
ϑ_A to ϑ_E	Range of the temperature transmitter

q	Flow
ϱ	Density
Δp	Active pressure
p	Pressure
ϑ	Temperature (°C)
T	Temperature (K)
V	Specific volume
K	Flow coefficient
R	Gas constant
F	Correction factor f (p, T)

Indices:

A	Start
E	End
B	Calculation state
abs	Absolute variable
m	Ground
v	Volume

Figure 1–27 Display of the correction range

This gives for the corrected flow

$$q = F \cdot K \cdot \sqrt{\varrho_B} \cdot \sqrt{\Delta p} = K \cdot \sqrt{\varrho_B} \cdot \sqrt{\Delta p} \cdot \sqrt{\frac{T_B \cdot p}{P_B \cdot T}}$$

The factor contained in the formula $K \cdot \sqrt{\varrho_B}$ is already taken into account in the measurement of the active pressure and can therefore be ignored by the computer.

Related to the correction factor it follows:

$$A = \sqrt{\Delta p} \cdot \sqrt{f\,(E2,\ E3)} \text{ with } F = \sqrt{f\,(E2,\ E3)} = \sqrt{\frac{(PE - PA)\ E2 + PA}{(tE - tA)\ E3 + tA}}$$

The measuring ranges are normalized to the calculation state with the parameters PA, PE, tA, tE (correction quotients start/end for pressure and temperature).

Mass flow computer, qm

$A = q_m,\ E2 = p,\ E3 = \vartheta$

$$PA = \frac{P_{absA}}{P_B},\quad PE = \frac{P_{absE}}{P_B},$$

$$tA = \frac{T_A}{T_B},\qquad tE = \frac{T_E}{T_B} \text{ with } T_{A/E/B}\ [K]$$

Volume flow computer related to the operating status q_V

Since the volume is reciprocally proportional to the density, a volume flow computer can be made out of this mass flow computer by changing the inputs E2 and E3.

$A = q_v,\ E2 = \vartheta,\ E3 = p$

$$PA = \frac{T_A}{T_B},\quad PE = \frac{T_E}{T_B} \text{ with } T_{A/E/B}\ [K],$$

$$tA = \frac{P_{absA}}{P_B},\quad tE = \frac{P_{absE}}{P_B}$$

Volume flow computer related to the standard status q_{VN}

Since the output signal is now related to the volume flow in the standard status, T_N = 273.15 K, P_N = 1.01325 bar_{abs} and no longer to the operating state, it must be corrected accordingly.

$A = q_{VN},\ E2 = p,\ E3 = \vartheta$

$$tA = \frac{T_A}{T_B},\qquad tE = \frac{T_E}{T_B} \text{ with } T_{A/E/B}\ [K],$$

$$PA = \frac{P_{absA}}{P_B},\quad PE = \frac{P_{absE}}{P_B}$$

The following applies for all computers:

p_{absA} to p_{absE}	Transmitter range absolute pressure (bar)
T_A to T_E	Transmitter range absolute temperature (K) is formed from the transmitter range ϑ_A to ϑ_E by conversion: T(K) = 273, 15 + ϑ (°C)

p_B, T_B Pressure and temperature of the calculation state of the measuring panel (absolute values)

p_B and T_B must be within the ranges of the transmitters; and may not be more than the factor 100 away from the range limits.

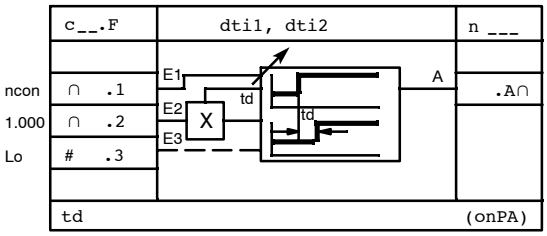
PA, tA = 0.01 to 1

PE, tE = 1 to 99.99

The input C**.1 $\sqrt{\Delta p}$ is limited to the values $\geq$ 0.

If the adjustable ranges for PA, PE, tA, tE are not adequate, a linear equation can be switched before the appropriate input for adaptation (function block LinE, see chapter 1.5.6, page 38).

Dead time element dti1, dti2



The input function E1 is displayed at the output delayed by the time td (dead time 1 to 9984 s). This time can be multiplied by a factor E2 and therefore changed externally.
The dead time element is implemented as a cyclic memory with 100 memory locations. The spacing between the input and output time represents the dead time.
If td = oFF the input is connected through without time delay.
If td $\leq$ 200 tc (tc cycle time), both pointers are moved cyclically, i.e. the cyclic memory is written and read per cycle.
If td $>$ 200 tc the pointers are only moved every nth cycle, the cyclic memory is written and read correspondingly less. To prevent „spot measurements", the input value is averaged over the input pointer movement.

The number of stored values is $n = \frac{td}{tc}$ n integer, rounded up or down and $\leq$100.

If the digital input c**.3 is high, the dead time element is blocked, i.e the output holds its momentary value and further input data are not stored (reaction like halted conveyor belt). When the digital input returns to low, the input data available before the blocking point are output. The applied input values are stored again.

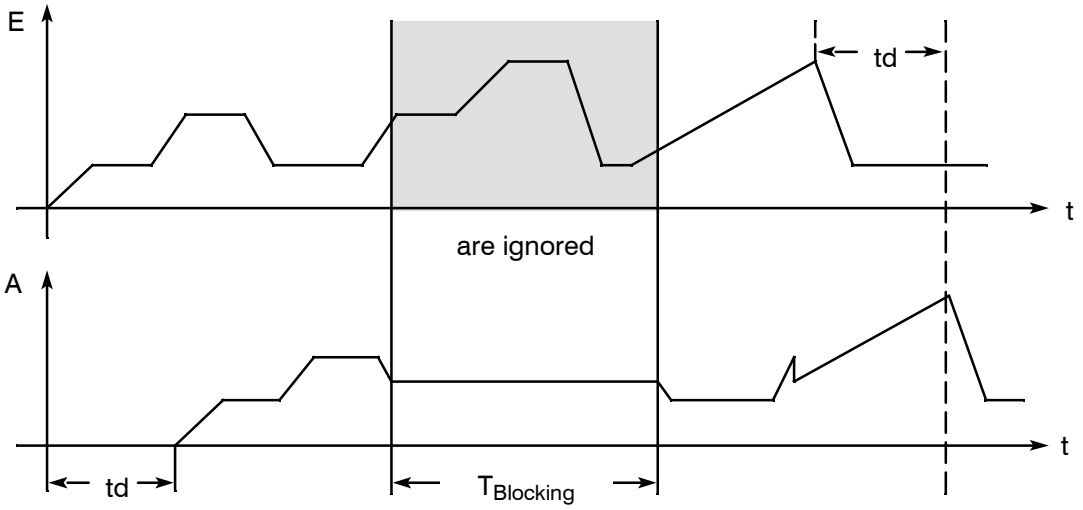
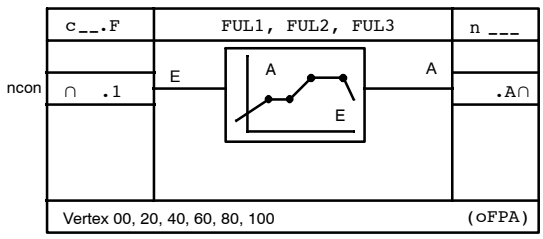


Figure 1–28 Timing function, dead time element

Restart conditions:

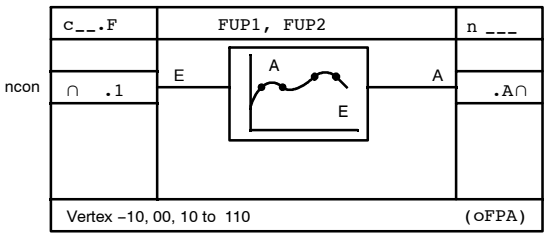
Power on	Band B
bAtt = no	0.000, until td runs out
bAtt = YES (hdEF)	last value until td runs out

Function transmitter FUL1, FUL2, FUL3 (linear)



The function transmitter assigns every value of the input variable E in the range from 0 % to +100 % an output variable A in the range from –199.9 % to +199.9 % by means of the function entered by the user: A = F(E). The function is entered by the private parameters „vertex 00 to 100 for 0 % to +100 % E in 20% steps. The function is continued linearly when E overmodulates.
The output function is formed by linear sections between the vertexes.
The function transmitters can be used for example for parameter control in the controller function blocks h*.F.

Function transmitter FUP1, FUP2 (parabola)



The function transmitter assigns every value of the input variable E in the range from –10 % to +110 % an output variable A in the range from –199.9 % to +199.9 % by means of the function entered by the user: A = F(E). The function is entered by the private parameters „vertex –10 ... 110" for –10 % to +110 % E in intervals of 10 %. Parabolae are set by the computing program between these vertex values which interlink tangentially the vertex values so that a constant function is produced. The vertex values at –10 % and +110 % E are required for the overflow. The last rise remains constant in the case of further overmodulation of E. When using as a linearizer for the indicators the linearization function is input by the 13 vertex values so that the multiplication function gives a linear equation.

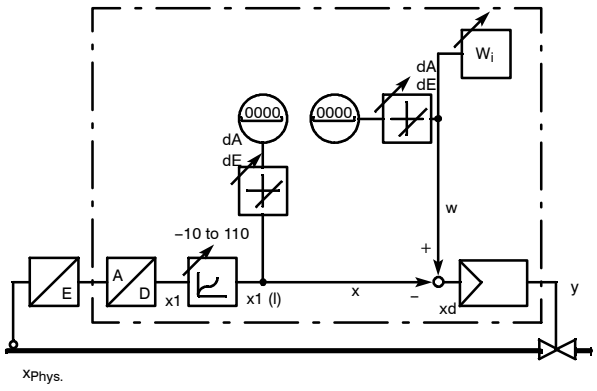


Figure 1–29 Using of function transmitter to linearize non–linear process variables for the display and control

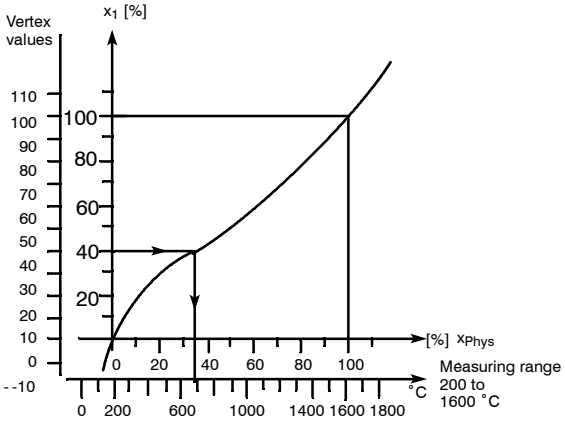


Figure 1–30 Sensor function e.g. from table

Example: Linearization of the controlled variable x1

The vertex values 0 and 100 are set with 0 % and 100 % so that x_1 (I) is available again as the normalized variable and the reference points for the definition of the display range of the x display are correct (see chapter 1.5.3, page 29).

To determine the vertex values, apply the sensor function according to figure 1–30 to 1–32 (page 64) and divide the measuring range into 0 to 100 % (x_{Phys} in %). Then the vertex values at –10 % to +110 % x on the x_{Phys} axis are read in % and input one after the other in the configuring mode oFPA.

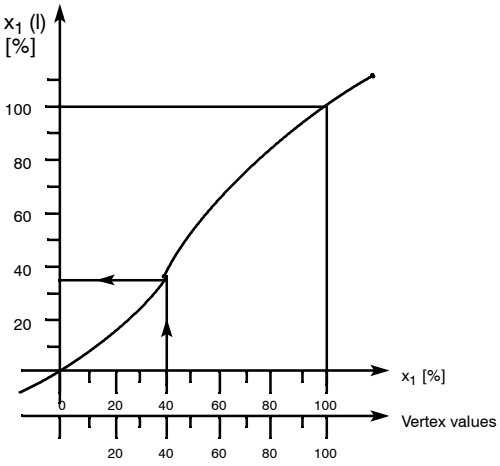


Figure 1–31 Linearization function

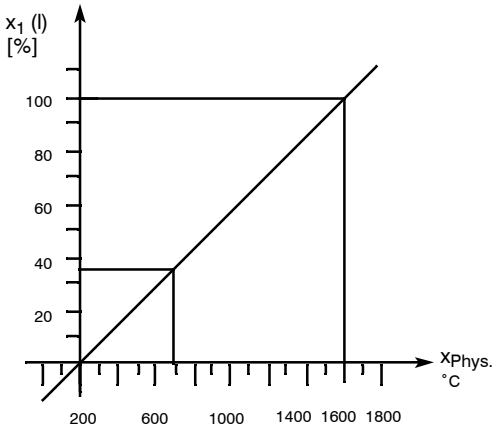
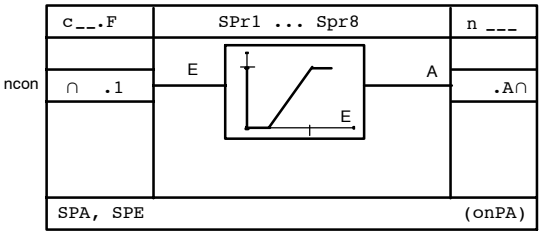


Figure 1–32 Linearized controlled variable x1(l)

Split range SPr1 to SPr8



The split range function consists of a linear equation between foot point SPA (output value 0) and corner point SPE (output value 1).

An output limiting to 0 or 1 takes place outside this range. Both a rising and a falling branch can be implemented by setting the two private parameters onPA SPA, SPE.

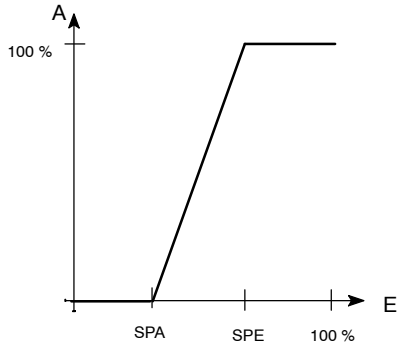


Figure 1–33 SPA < SPE => rising

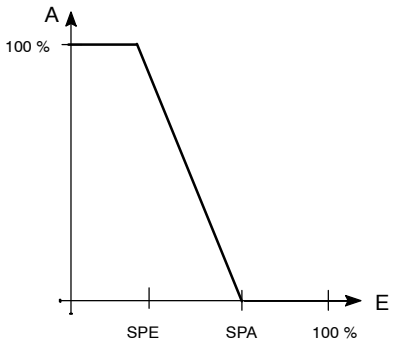
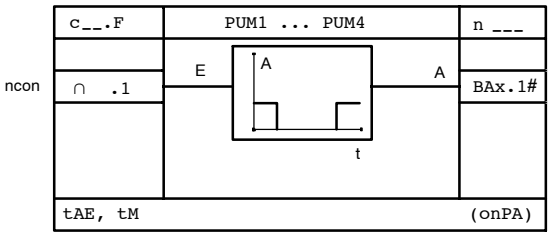


Figure 1–34 SPA > SPE => falling

Pulse width modulator



Example:

Input value: 0.3
Period: 4 s
=> Turn–on time 1.2 s
Pause 2.8 s

The pulse width modulator converts an analog signal into a pulse width modulated digital signal.
Private parameters (onPA): tM Period
tAE Minimum turn–on time

PUM1 –> BA1.1
PUM2 –> BA2.1
PUM3 –> BA3.1
PUM4 –> BA4.1

CAUTION

possible collision with Csix/Csex!
–> binary outputs BA1 ... 4 for ± Δy

1.5.8.3 Arithmetic Blocks d01.F to d04.F

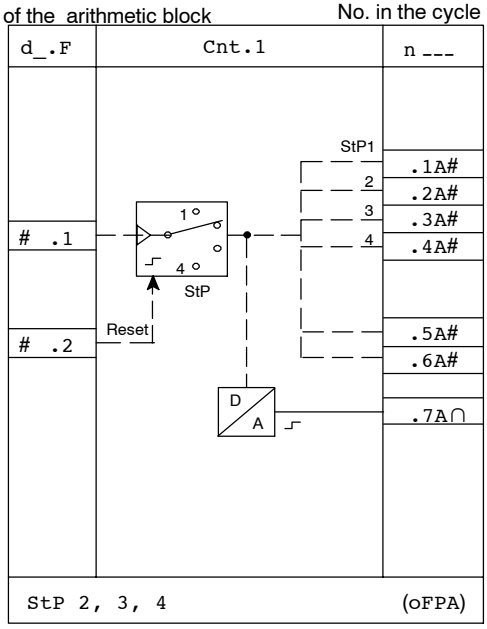
Consecutive number of the arithmetic block

No. in the cycle

d0_.F	Name of the arithmetic block	n ___
.01		
.02		
.03		.1A
.04		.2A
.05		.3A
.06		.4A
.07		.5A
.08		.6A
.09		.7A
.10		.8A
.11		.9A
.12		.10(A)
		.11(A)
		.12(A)
		.13(A)
		.14(A)
Private parameters		

Consecutive number of the arithmetic block

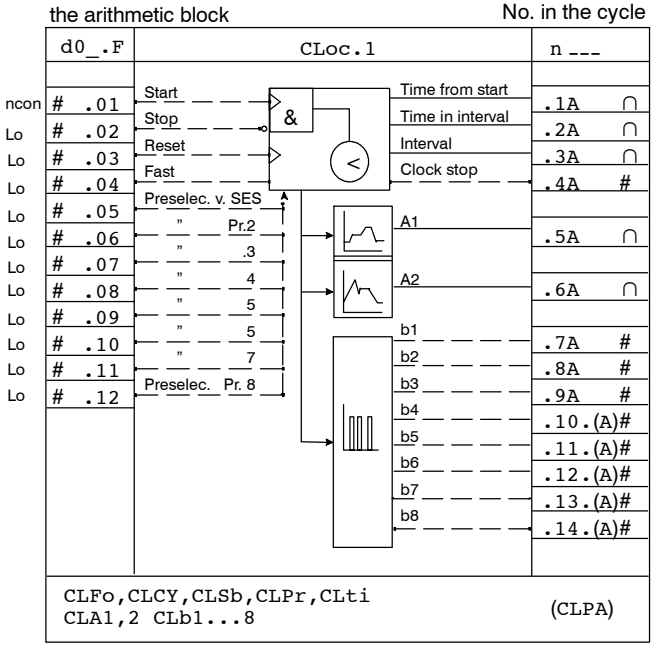
No. in the cycle



Demultiplexer

Consecutive number of the arithmetic block

No. in the cycle



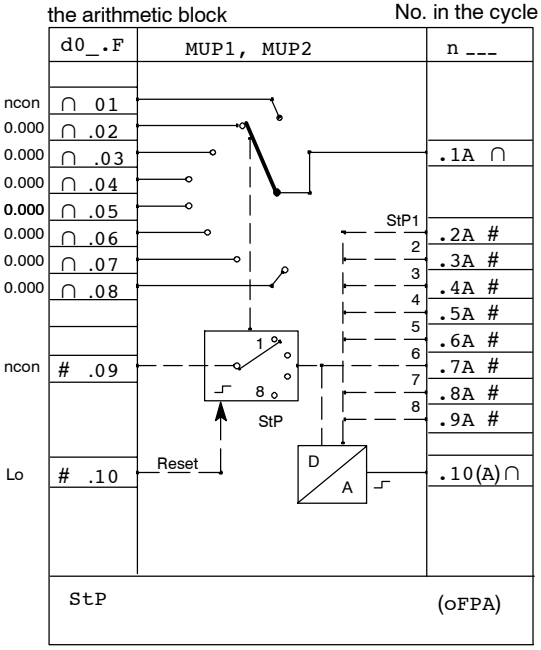
Clock

∩ = analog

= digital

Consecutive number of the arithmetic block

No. in the cycle



Measuring point switch (multiplexer)

In the arithmetic blocks, the demultiplexer Cnt1 and the clock 1 can be defined once, the measuring point switch MUP twice. Below the demultiplexer, the clock and the measuring point switch are explained in detail.

Demultiplexer Cnt1

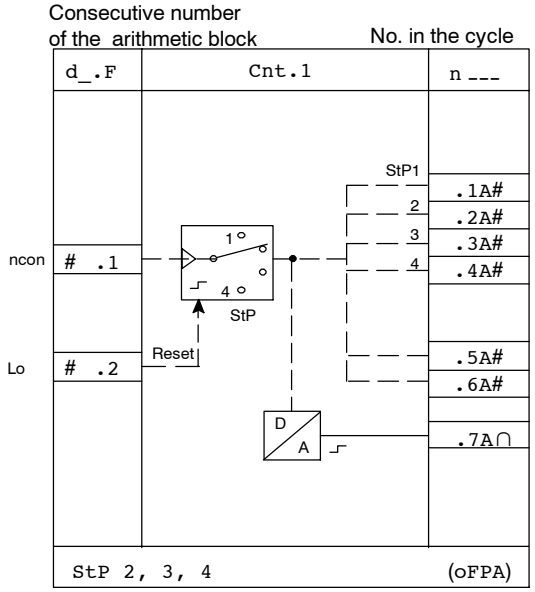
The demultiplexer can be defined once in FdEF in the arithmetic blocks d0*.F. The counter reading is output with the demultiplexer binary coded according to the table below. Further switching takes place edge–controlled at the clock input d*.1 (switching in closed loop, limited by private parameter StP).

The counter can be driven with a high signal through the reset input d*.2. The position can be displayed by connecting the output with the display dd3.

This block serves above all for display and key switching in multiple controllers (max. 4)

Example:

- Counter switching Cnt1, e.g. with tA6.1
- Connecting the outputs d*.5/d*.6 with dd*.U/dd*.M (*: 1 to 3) and L10.1/L11.1
  By switching over, the appropriate controller signals setpoint w, actual value x, manipulated variable y are switched over.
  The selected controller can be detected at the LED display.

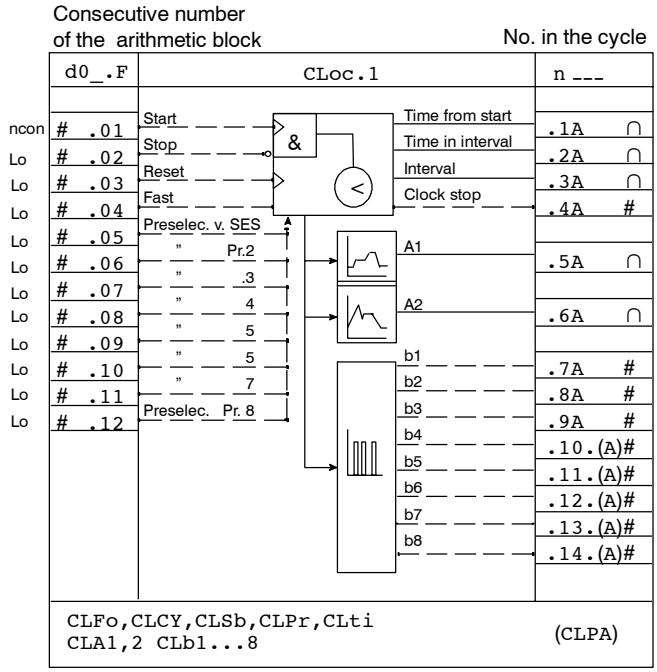


StP	1A	2A	3A	4A	5A	6A
1	1	0	0	0	0	0
2	0	1	0	0	1	0
3	0	0	1	0	0	1
4	0	0	0	1	1	1

Note:

- see example in chapter 7.5, page 191

Clock CLoc



The clock can be defined once in FdEF in the arithmetic blocks d0*.F. Two analog outputs and 8 digital outputs can be assigned to a common timebase – with a maximum 40 time intervals – with the clock.

These 40 intervals can be distributed between up to 8 independent sub–routines. An appropriate number of intervals is assigned to the programs CLPr 1 to 8. (parameter CLPr).

The time intervals of the programs are entered per interval according to the selected clock format (private parameter CLFo) in [h, min] or [min, s] (private parameter CLti). Then the time intervals are assigned the values for the analog outputs (private parameter CLA*) or the status of the digital outputs (private parameter CLb*). The programs defined in CLPr can run once, several times or cyclically (private parameter CLCY). The clock process can be accelerated in steps for test purposes (private parameter CLSb). The clock is controlled by the inputs Start, Stop, Reset and Fast.

The controlling source for the program preselection is defined with d*.05.
d*.05 = low preselection through the inputs d*.06 to d*.12
d*.05 = high preselection through the SES (Status ST–CLOCK)

If the inputs d*.06 to d*.12 are low, the 1st program runs after Start. A high signal at one of the preselection inputs d*.06 to d*.12 defines the program 2 to 8 to be processed which is activated with the edge Start = Low/High. The time process can be monitored by the outputs time from Start, time in the interval, interval display and Clock stop.

The following components are described in detail below:

- Private parameters
- Inputs d*.01 to d*.12
- Outputs d*.1A to d*.14.(A)

- **Private parameters**

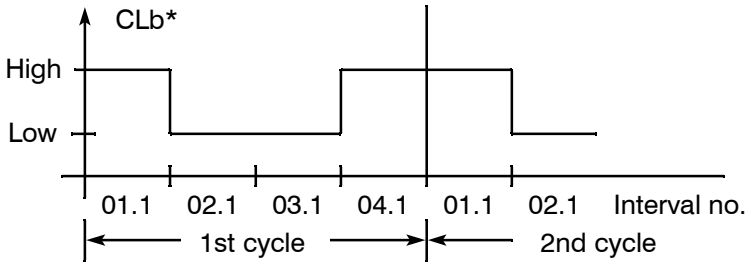
  Because of the large number of clock parameters, these are set offline in their own mode (CLPA) (see chapter 3.3.4, page 148). This applies for all programs Pr. 1 to Pr. 8.

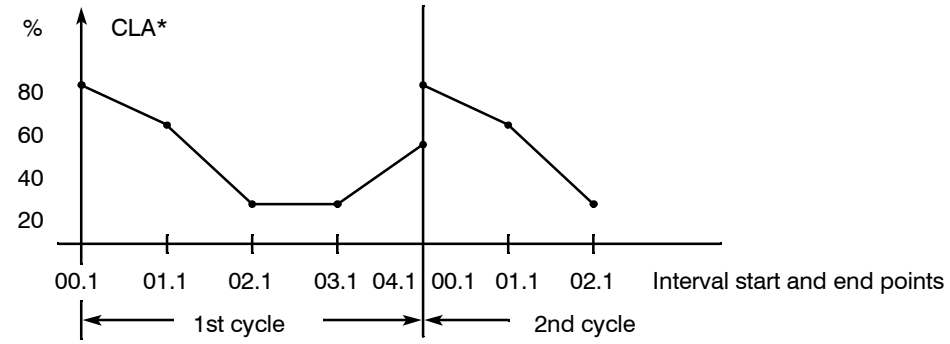
  - **CLFo clock format**
    The desired clock format (0 h.0' or 0'.0") is specified for all programs together with CLFo with which the time per interval is set in CLti.

  - **CLSb factor for clock fast action**
    The time process can be accelerated by the factor set with CLSb through the input d*.04 (Fast) = high for test purposes. It should be taken into account when selecting the acceleration factor that the linear equations are adequately resolved by the computing cycle time. The factor is valid for all programs.

Acceleration factor	Time procedure for ... . in			
	1 week	1 d	1 h	1 min
360	28 min	4 min	10 s	–
168	60 min	–	–	–
120	84 min	12 min	30 s	0.5 s
60	168 min	24 min	1 min	1 s
24	7 h	1 h	2.5 min	2.5 s
12	14 h	2 h	5 min	5 s
6	28 h	4 h	10 min	10 s
3	56 h	8 h	20 min	20 s

  - **CLCY Number of program cycles**
    The number of program cycles can be set from 1 to 255 or cyclic run (CYCL) with CLYC. A program cycle is processed at the end of the last interval of the selected program. When this point has been run according to the set number of program cycles, the clock stops (output d*.4A (Clock Stop) = High) and must be restarted to continue. If d*.3A (interval display) is switched with dd3, the decimal point of the display flashes with the clock at standstill. When the program runs several times the loop from the end of the last interval to the start of the 1st interval is closed. It should be noted that in the transition from the end of the last to the start of the 1st interval a jump takes place in the analog value if equal values are not set for these points. (See – CLA1, 2)
    At t = 0 of the 1st interval the digital outputs adopt the status of the 1st interval. CLCY is valid for the respective selected program.





t = 0 of the 1st interval

Interval	CLA...	CLb...		Meanings interval display at CLA	at CLb
00.1	80 %	–	↑	Start 1st interval (t = 0)	–
01.1	60 %	High	↑	End 1st interval	1st interval
02.1	20 %	Low	1st program	End 2nd interval	2nd interval
03.1	20 %	Low	↓	End 3rd interval	3rd interval
04.1	50 %	High	↓	End 4th interval	4th interval

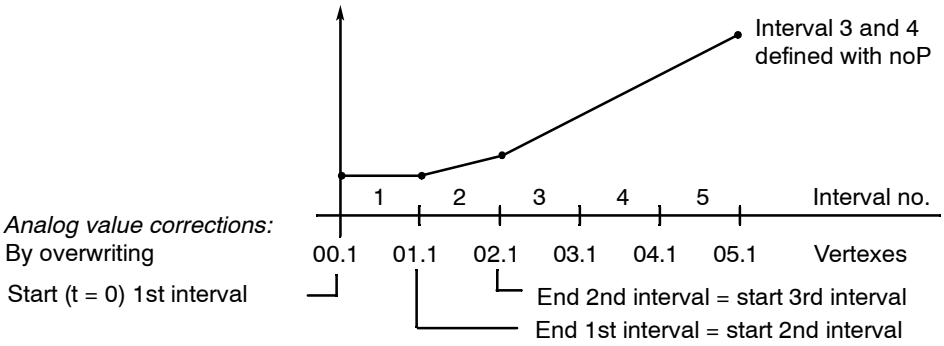
Interval no. in the display dd3
Program no.

- **CLPr program interval assignment**
  The number of intervals is assigned to the individual programs _ _.1 to _ _.8 with CLPr. The number of intervals is individually adjustable and limited to 40 in total over all programs. In addition the adjustment is blocked. (Factory setting is no.1 to no.8, i.e. no interval is assigned to the programs 1 to 8.)
  Corrections:
  It is possible to correct the number of intervals of a program. If the number of intervals is reduced the data of the omitted intervals are deleted, (CLti, CLA1, CLA2, CLb1 to CLb8) the parameter data of the remaining intervals are retained.
  On increasing the number of intervals, the parameters of the new intervals are offered with factory setting, whereas the parameters of the already defined intervals of this program are retained.
  The factory setting of all parameters of a program is obtained by first deleting the program by selecting „no” and then specifying the desired number of intervals.
  Other programs remain unchanged.

- **CLTi time interval setting**
  The intervals assigned to the programs in CLPr initially have factory setting (minimum time 00.01). The times are entered as Δt according to the set clock format in h/min or min/s.
  This means: 01.n 1st interval of the program n
  02.n 2nd interval of the program n
  with n = 1 to 8 and the max. possible interval number 1 to 40 over all programs

  If d*.3A (interval display) is wired with dd3, the appropriate intervals are didplayed in on-line mode.
  Corrections:
  Time corrections are made by changing the times in CLti.

- **CLA1, 2 analog output function**(amplitude default)
  Two independent output functions can be assigned to the common time base with CLA1 and CLA2. The functions are composed of linear sections. In the 1st interval of the respective program n, the input of the start value for t = 0 (00.n) and the end value (01.n) for the 1st linear section of the program n is necessary. In the other intervals only the end values are entered for the sections of the polygon line. The end values are at the same time start values for the next interval. If an interval is occupied by noP (no operation), the analog value is calculated as an intermediate value of the adjacent vertexes in this interval. If the 1st value 00.n is occupied by noP, no analog output CLA1, 2 is possible for this program, 0 % is output.



- **CLb1 to CLb8 digital status in the interval**
  Eight independent digital outputs CLb1 to CLb8 can be assigned to the common time base.
  The status, Low or High, is entered in the displayed interval.
  Status corrections:
  By overwriting

- **Configuring**
  The clock is at a standstill during configuring. It must be restarted according to the start condition from the start of the program after exiting the mode CLPA, hdEF, FdEF, FCon and FPoS when changes are made in the configuring. Without changes, the clock continues running from the interrupt when entering OnPA or the process operation mode.
  The clock continues running during the parameterization mode.

- **Power failure**
  The clock stops running in the event of a power failure!

Restarting after a power failure

Power ON	Reaction
bAtt = no	Clock goes to t = 0 of the 1st interval of the selected program and stops
bAtt = YES (hdEF)	Clock continues running from $t_{power\ off}$

- **Inputs d*.01 to d*.12**

Input				Output	Remarks
Start d*.01	Stop d*.02	Res d*.03	Fast d*.04	Clock stop d*.4	
x	x	↑	x	1	Reset to start of selected program
x	1	0/1	x	1	Start blocked, clock stopped
↑	0	0/1	0	0	Clock running time synchronously
0/1[1)]	0	0/1	1	0	Clock runs with acceleration factor

↑ = rising edge
x = no effect
* = consecutive number of the block d
1 = High
0 = Low
1) Clock must be started

- **Start d*.01**
  Every positive edge at d*.01 starts the clock and thus the program selected by the preselection inputs (see there), if d*.02 (stop) = low. Start takes place after reset and end of the program with the time t = 0 of the 1st interval
  After clearing the stop function, the start edge continues the program from the state which existed before the stop function. If several preselection inputs d*.06 to d*.12 are occupied with high or a selected program has no intervals, the clock is not started.

- **Stop d*.02**
  With d*.02 = Hi the clock is stopped, the output d*.4A (Clock Stop) becomes Hi, the analog and binary outputs d*.5A to d*14(A) retain their values, the input d*.01 (Start) is blocked. If d*.3A (interval display) is switched with dd3, the decimal point of the display flashes in the stop function.

- **Reset d*.03**
  Every positive edge at d*.03 sets the clock to t = 0 of the 1st interval of the program selected with the preselection inputs (see there). The clock is at a standstill and the output d*.4A is high. If d*.3A (interval display) is switched with dd3, the decimal point of the display flashes. At t = 0 of the 1st interval, the binary outputs adopt the status of the 1st interval, the analog outputs go to the value at time t = 0 of the 1st interval.

  Power on (at bAtt = no), manual reset and all changes in the configuring automatically trigger the reset for the clock.

- **Fast d*.04**
  The clock runs time synchronously at d*.04 = Low and at d*.04 = High with the set acceleration factor (see CLSb) if it was started previously by d*.01.

- **Source for the program preselection d*.05**
  AT d*.05 = Low preslection is made through the inputs d*.06 to d*.12, at d*.05 = High the preselection is made through the serial interface SES (Status SI–CLOCK).

- **Program preselection d*.06 to d*.12**
  Program preselection through digital inputs, at d*.05 = Low:
  d*.06 to d*.12 determine the program according to the following table:

d*.12	d*.11	d*.10	d*.09	d*.08	d*.07	d*.06	Program
Lo	Lo	Lo	Lo	Lo	Lo	Lo	1
Lo	Lo	Lo	Lo	Lo	Lo	Hi	2
Lo	Lo	Lo	Lo	Lo	Hi	Lo	3
Lo	Lo	Lo	Lo	Hi	Lo	Lo	4
Lo	Lo	Lo	Hi	Lo	Lo	Lo	5
Lo	Lo	Hi	Lo	Lo	Lo	Lo	6
Lo	Hi	Lo	Lo	Lo	Lo	Lo	7
Hi	Lo	Lo	Lo	Lo	Lo	Lo	8

  The preselection inputs must have reached the desired level before start or reset. Level changes during the program run have no influence. If more than one input d*.06 to d*.12 has Hi level or the selected program n is not defined (CLPr = no.n), the clock does not start with the start edge. If d*.3A (interval display) is switched with dd3, no.n is displayed after start or reset in this error case. The error must be cleared and the program re-started.

- **Outputs d*.1A to d*.14.(A)**

  - **d*.1A Time from start 1st interval of a program**
    Only for direct connection with dd1.1 to dd2.2. Only these connections are permitted in the FCon mode. The private parameters of the displays are not effective. The time in h, min from the start of the 1st interval is displayed. At 23.59 the clock switches to 00.00. It is reset by Reset (d*.03), see under Reset d*.03.

  - **d*.2A Time in interval**
    Only for direct connection with dd1.1 to dd2.2. Only these connections are permitted in the FCon mode. The private parameters of the displays are not effective. The time in the currently running interval is displayed in min, sec or h, min depending on CLFo.

  - **d*.3A interval**
    Only for direct connection with dd3.1 and dd3.2. Only these connections are permitted in the FCon mode. The private parameters of dd3 are not effective.
    The current interval xx and the running program n in the form xx.n are displayed.
    The display of the interval is retained until the appropriate interval has run out.

  - **d*.4A Clock Stop**
    The output is always high when the clock stops. This is the case after Stop, Reset, Power on (with batt = no.), manual reset and at the end of the program cycle.

  - **d*.5A, d*.6A Analog outputs A1, A2**
    Outputs of the analog values A1 (d*.5A) and A2 (d*.6A), which are assigned to the intervals (see CLA1, CLA2).

- **d*.7A to d*.14 (A) digital outputs b1 to b8**
  Digital outputs b1 to b8 for the digital status signals assigned to the intervals (see CLb1 to CLb8).

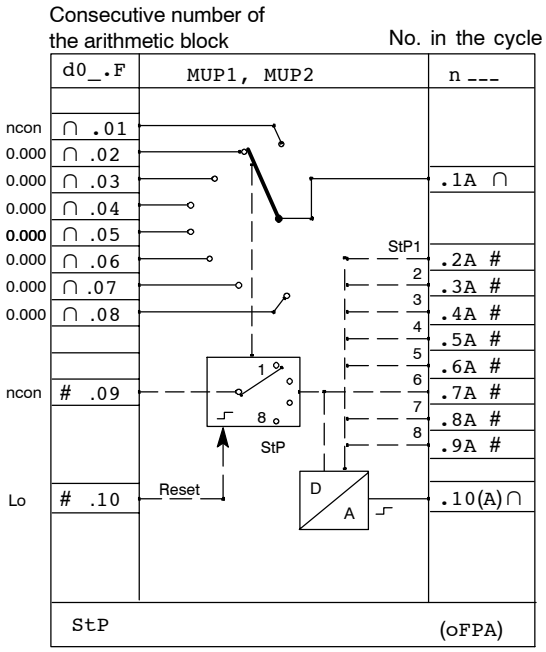
Measuring point switch (multiplexer) MUP1, MUP2

The measuring point switch can be defined twice in FdEF in the arithmetic blocks d0*.F. Up to 8 analog inputs can be connected through to one output (d*.1A) with the measuring point switch. Further switching takes place edge–controlled at the clock input d0*.9. (switching in closed loop). Every switching state is displayed by a high signal at a separate output (d*.2A to d*.9A) These signals can be linked with the preparation inputs of the clock and can select a specific process program there (for example). In addition the respective position can be displayed by connecting the output d*.10.(A) with display dd3. (Display format factory setting, display 1 to 8)

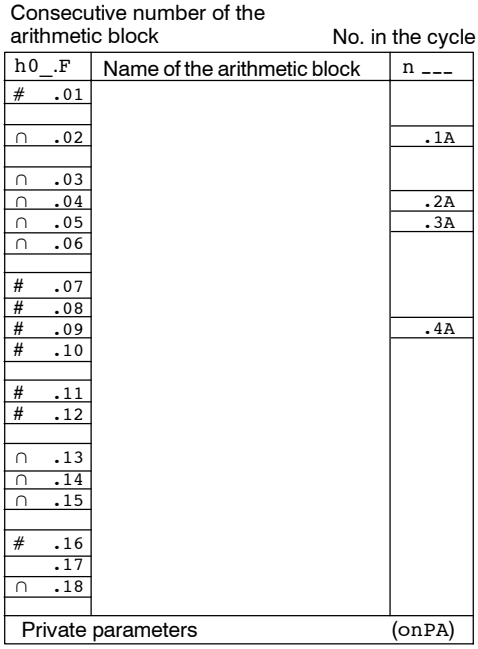
The maximum number of measuring points is selected with the private parameter StP (number of switching steps) (adjustable from 2 to 8); factory setting is 8. The multiplexer can be driven to position 1 by the reset input (d*.10) with a high signal.

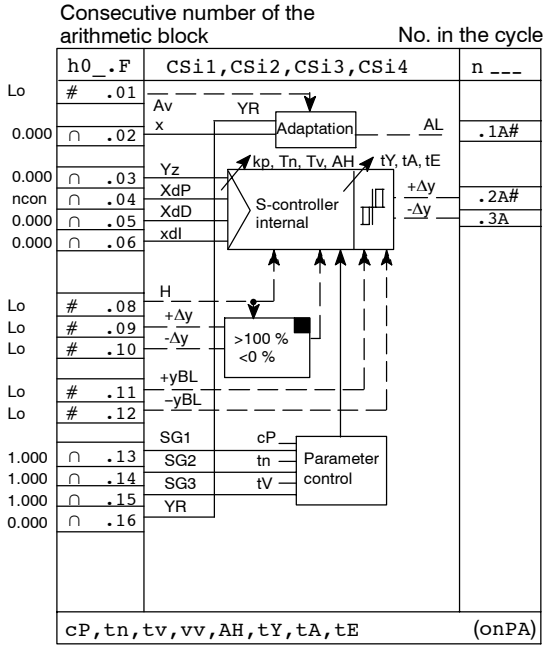
Restart conditions:

Power On	Outputs
bAtt = no	Switch position 1
bAtt = YES	Switch position retained

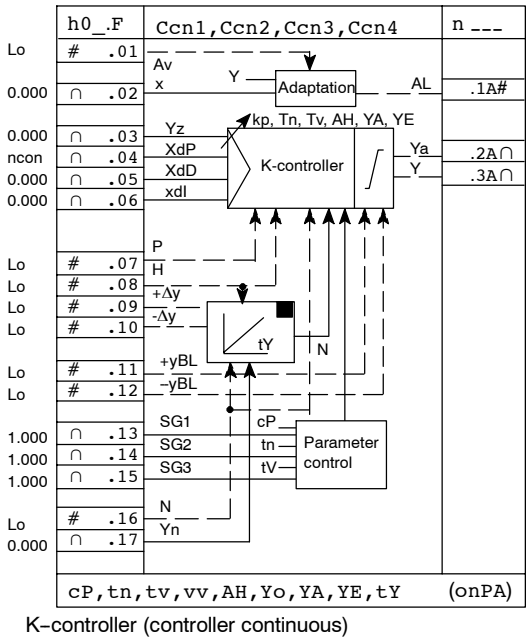


1.5.8.4 Arithmetic Blocks h01.F to h04.F

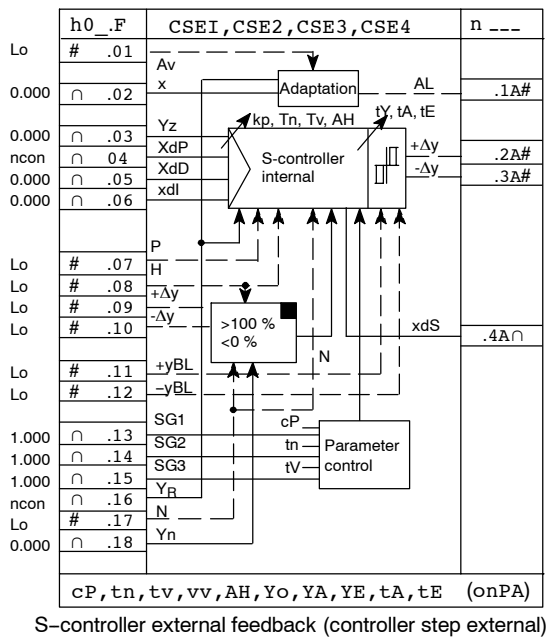




S controller internal feedback (controller step internal)



K–controller (controller continuous)



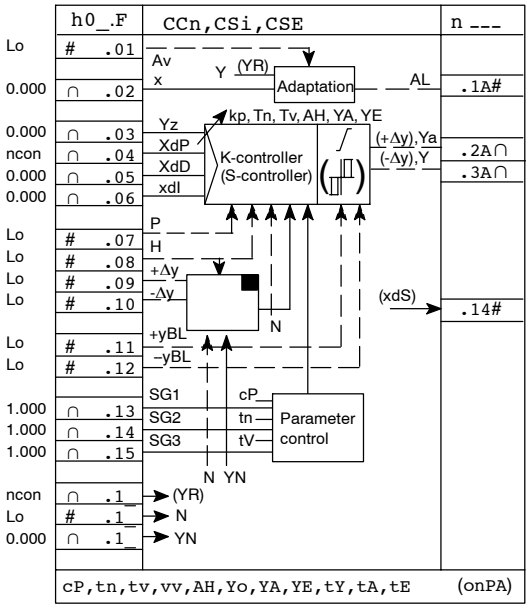
S–controller external feedback (controller step external)

∩ = analog
= binary

In the arithmetic blocks h*.F a total of 4 controller blocks can be defined in FdeF, optionally
K-controller 1 (Ccn1) or S-controller int 1 (CSi1) or S-controller ext 1 (CSE1) and
K-controller 2 (Ccn2) or S-controller int 2 (CSi2) or S-controller ext 2 (CSE2) and
K-controller 3 (Ccn3) or S-controller int 3 (CSi3) or S-controller ext 3 (CSE3) and
K-controller 4 (Ccn4) or S-controller int 4 (CSi4) or S-controller ext 4 (CSE4)
S-controller int = S-controller with internal position feedback
S-controller ext = S-controller with external position feedback

Figure 1–35 Arithmetic blocks h, controller

K-controller (Ccn*), S-controller internal (CSi*), S-controller external (CSE*)



The PID algorithm is implemented as a parallel structure with interaction–free parameter setting. The P, D, and I part have separate control difference inputs (xdP, xdD, xdI), the Z part is added to the output YA.

PI is switched over to P operation with the control signal P = High. Automatic mode is switched over to manual mode with the control signal H = Hi.

Manual actuation takes place through the control inputs $\pm\Delta y$ with a Hi signal (e.g. by pressing a key on the front). Blocking of the output through the digital inputs $\pm$YBL (blocking = High) is provided. The output of the controller is followed up by a control signal N = High to the input value applied at YN. (Only in K–controller and S–controller ext.)

Parameter control of the most important parameters kp, Tn, Tv by separate inputs SG1 to SG3 is possible. To do this, the basic parameter value cP, tn, tv set in onPA is multiplied with an external function.

The parameter adaptation is possible in offline mode of the respective controller for the parameters cP, tn, tv, vv and AH. The controlled variable x must be fed to the controller for this. If (CSi*) YR is switched internally with 0.000 or ncon in the S–controller, the value of the step command is determined from ty.

Then the adaptation can be run in manual mode (see the following description of the **adaptation** and chapter 3.3.2, page 138).

The following components are described in detail below

- Functional explanation of the digital control signals and inputs
- Control algorithm
- General parameters
- K-controllers Ccn1, Ccn2, Ccn3, Ccn4

- S–controllers with internal positioning feedback CSi1, CSi2, CSi3, CSi4
- S–controllers with external positioning feedback CSE1, CSE2, CSE3, CSE4
- Adaptation
- Adaptation of the S–controller to the actuating drive
- Automatic setting of the control parameters by the adaptation procedure
- Manual setting of the control parameters without knowing how the system will react
- Manual setting of the control parameters after the transient function

- **Functional explanation of the digital control signals and inputs**

P ***P-operation controller (h*.07)***
The Pi–controller is switched to P–operation with this signal.

H ***Manual (h*.08)***
This signals blocks the output of the controller and enables direct manual adjustment of the manipulated variable through the front operating mode with the appropriate wiring for example.

N ***Tracking***
With this signal the output of the K–controller and the three–position step controller with external position feedback is tracked to the tracking signal y_N.

$\pm\Delta y$ ***Incremental manipulated variable adjustment (h*.09, h*.10)***
External manipulated variable default for incremental adjustment through digital inputs in tracking operation.

yBL ***Direction–dependent blocking of the manipulated variable (h*.11, h*.12)***
Direction–dependent limiting of the manipulated variable by external signals, e.g. of the limit switches of the actuating drives. This limiting is effective in every operating mode.

- **Priority of the control signals Bl, N, H**
  Blocking has priority over tracking; tracking has priority over manual.
  This definition can be changed by external wiring with arithmetic blocks.

- **Control algorithm**

- **P-controller (control signal P = Hi)**

$ya = yp + yo + yz$

$ya = +kp \cdot xd_p + yo + yz$

Frequency response: $\frac{ya}{xd} = kp$

- **PI-controller**

$ya = yp + y_I(t) + yo + yz$

$$yI\,(t) + yo = \frac{kp}{Tn}\int_0^t xd_I\,dt + y_I\Big|_{t=0}$$

$$ya = kp\,xd_p + \frac{kp}{Tn}\int_0^t xd_I\,dt + y_I\Big|_{t=0} + yz$$

Frequency response: $\frac{ya}{xd} = + kp \left(1 + \frac{1}{j\omega\, Tn}\right)$

- **D-part**

  The D–part is added.

  Frequency response: $\frac{y_D}{xd_D} = + kp \frac{j\omega\, T_v}{1 + j\omega \frac{T_v}{V_v}}$

- **General parameters**

  - **Working point Yo for P controller**

    The working point yo of the P–controller can be set either automatically or as a parameter (onPA).

  - **Automatic working point (Yo = Auto)**

    Whenever there is no automatic operation (manual, tracking, safety or blocking operation) (yz is then active), the working point yo is tracked so that there is a bumpless switch over to the automatic mode.

    $yo = \overline{ya} - kp \cdot xdp - yz$

    This gives an automatic setting of the working point yo in manual mode:

    $yo = y_H - K_p\,(xd_H) - yz$ with $xd_H = w - x_H$

    If the actual value in manual mode (x_H) is driven to the desired setpoint (w) by the appropriate manual manipulated variable (y_H), the working point (yo) is identical to the manual manipulated variable (y_H).

    $yo = y_H$ or $yo = y_H + yz$

  - **Set working point (Yo = 0 to 100 %)**

    The controller operates in all operating modes with the working point set as a permanent parameter.

  - **Response threshold AH**

    The response threshold AH (dead zone element) is circuited after the inputs yz, xd_P, xd_D, xd_I in the control difference.

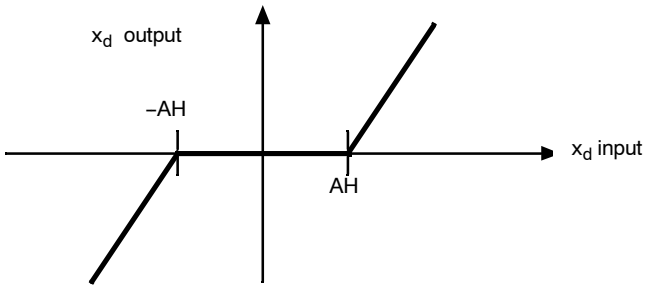


Figure 1–36 Effect of the dead zone element

The dead zone element lends the controller a progressive behavior, at small control differences the gain is low or even 0, at larger control differences the specified kp is reached. It should be taken into account that the remaining control difference can adopt the value of the set response threshold AH. The factory setting of AH is 0 % and can be set up to 10 % in the parameterization mode onPA.

In S-controllers the minimum necessary setting of AH is given by the minimum with $\Delta x = ks \cdot \Delta y$ and thus from the setting of tE. It can be increased to further calm the controlled system. A low response threshold of about 0.5 % is recommended in K-controllers to calm the control circuit and reduce wear on the actuator.

- **Manipulated variable limiting yA, yE**

  The manipulated variable limiting with the YA and YE parameters is only effective in automatic mode. The limits of these parameters are at –10 and +110 %. However, it should be taken into account that the controllers neither output negative actuating currents nor detect any negative position feedback signals.

  If the manipulated variable y_a reaches one of the limits YA or YE in automatic mode, further integration is aborted to avoid integral saturation. This ensures that the manipulated variable can be changed immediately after reversing the polarity.

  In manual or follow–up mode the manipulated variable y can be driven out of the limit range. When switching to automatic mode the last manipulated variable is transfered bumplessly, then only changes in the manipulated variable in direction of the range YA to YE are executed.
  The manipulated variable limiting is only possible in K-controllers and three–position step controllers with external position feedback.

- **Bumpless switching to automatic mode**

  If there is no automatic operation (manual, tracking or active blocking operation, active y = $y\overline{a}$), the I part or the working point yo (only when Yo = Auto) is tracked so that switchover to automatic operation (active y = ya) is bumpless. Any still active D part is set to zero.
  yI or yo = $y\overline{a}$ – kp · xd – yz then ya = $y\overline{a}$

- **P–PI switching**

  With the control signal P = 1 the controller is switched over from Pi to P behavior, at Yo = Auto the switchover by setting yo and $yy_I(t)$ is bumpless in both directions. If a fixed operating point yo is used, only switchover in direction of PI operation is bumpless.

- **Parameter control, inputs h*.13, h*.14, h*.15**

  With the control inputs SG1, SG2, SG3 the parameters Kp, Tn, Tv can be changed by an applied controlling variable.
  The following applies: Kp = cP · SG1, Tn = tn · SG2, Tv = tv · SG3
  The parameters kp, Tn, Tv gained in this way can be adjusted within the limits valid for the parameters cP, tn, tv.
  Typical controlling variables are the control difference xd (as an amount) for progressive controls and x or y for working point dependent controls (unilinear control lines). In addition it is possible to operate for example with great kp for startup procedures in P operation (control signal P = 1) and to control with reduced Kp after switching over to PI operation (control signal P = 0). The controlling variables can be switched over at the same time as P switchover.

The signal applied to the control inputs can be specified for example by the function transmitter FUL as a curve line.
The parameter values and the value of the controlling variable can be gained by adaptation (see under adaptation).

- **Restart conditions**

Power on	yp	YO		$Y_{It = 0}$	y_D	yz
		Auto	0 ... 100 %			
bAtt n = no	kp · xdP	-kp · xdP - yz	0 ... 100 %	-kp · xdP - yz	0 %	yz
bAtt = YES	kp · xdP	y_L - kp · xdP - yz	0 ... 100 %	y_L - kp · xdP - yz	0 %	yz

This gives for the manipulated variable in automatic mode ya when turning on:

Power on	PI(D) controller	P(D) controller yo = Auto	P(D) controller yo = 0...100 %
bAtt n = no	10 %	10 %	kp · xdP + yo + yz
bAtt = YES	y_L	y_L	kp · xdP + yo + yz

y_L = last manipulated variable before turning off

If other startup conditions are desired, the startup behavior can be influenced specifically by additional connection, e.g. x–tracking and tracking operation if necessary as a function of the data source rES1, rES2.

- **K-controllers Ccn1, Ccn2, Ccn3, Ccn4 (controller continuous)**

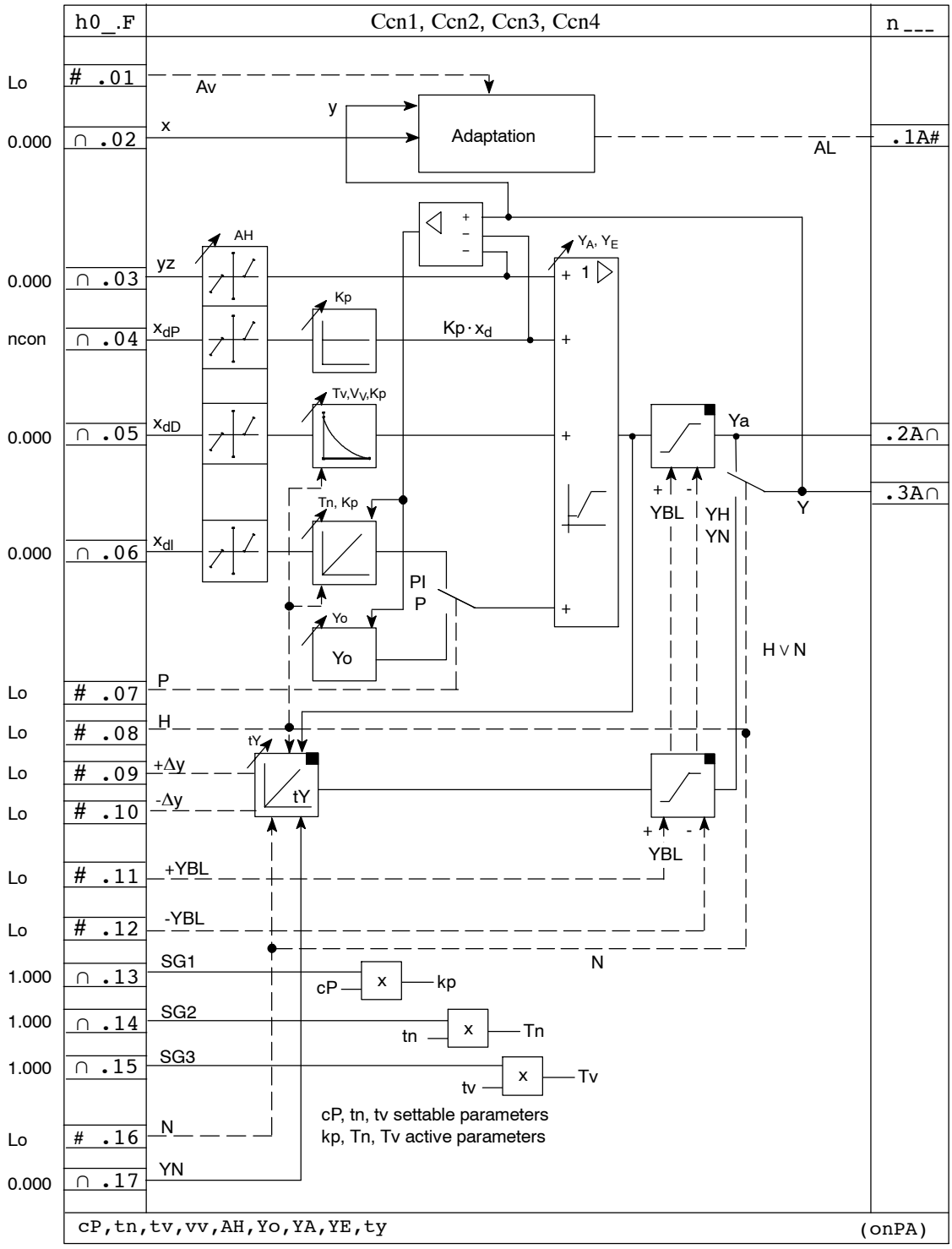


Figure 1–37 Arithmetic block h, continuous controller

- **S-controllers with internal positioning feedback CSi1, CSi2, CSi3, CSi4 (controller step internal)**

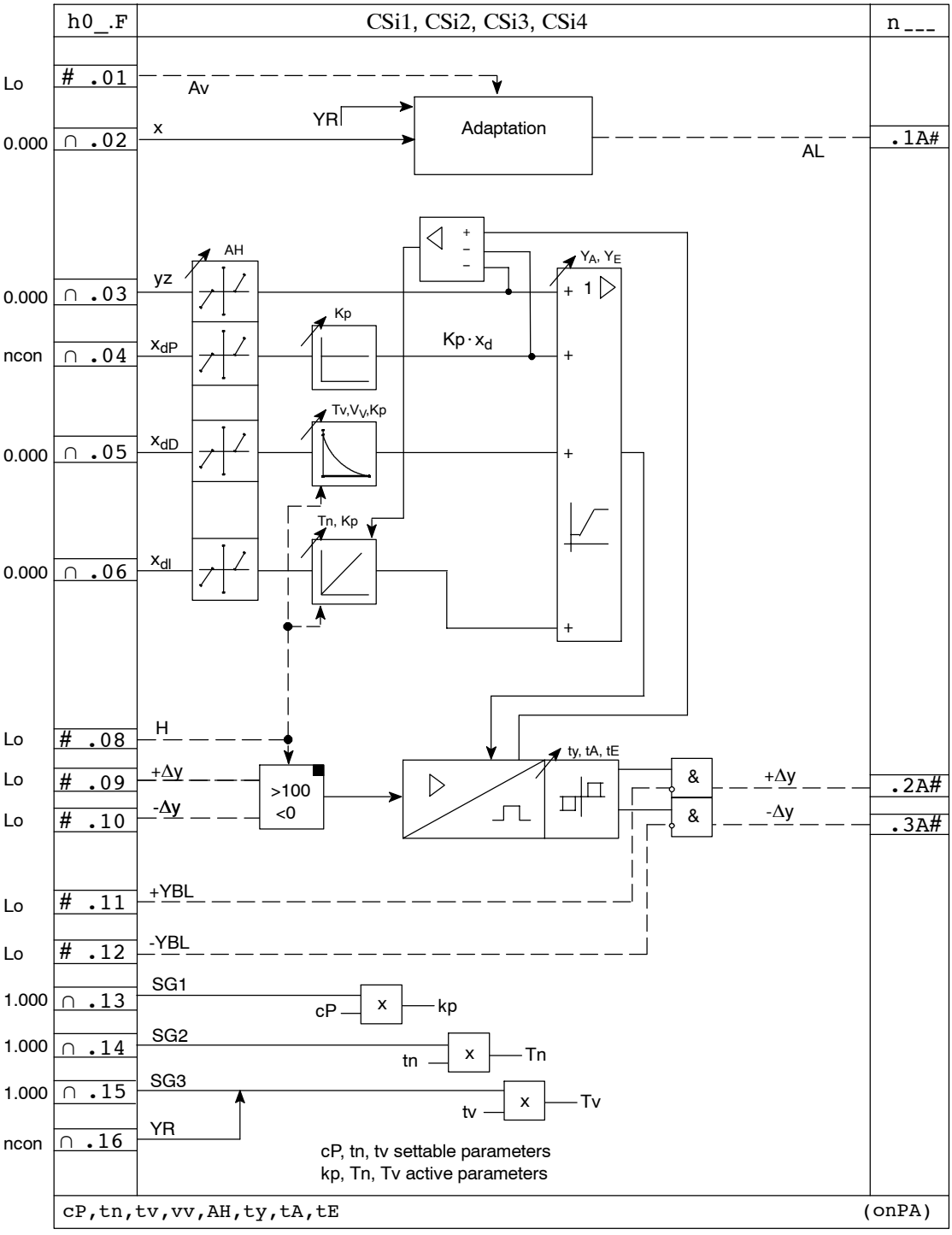


Figure 1–38 Arithmetic block h, S–controller with internal position feedback

Note: The manipulated variable outputs +Δy and −Δy are permanently assigned to the digital outputs (see chapter 1.5.3, page 29).

- **S-controllers with external positioning feedback CSE1, CSE2, CSE3, CSE4 (controller step external)**

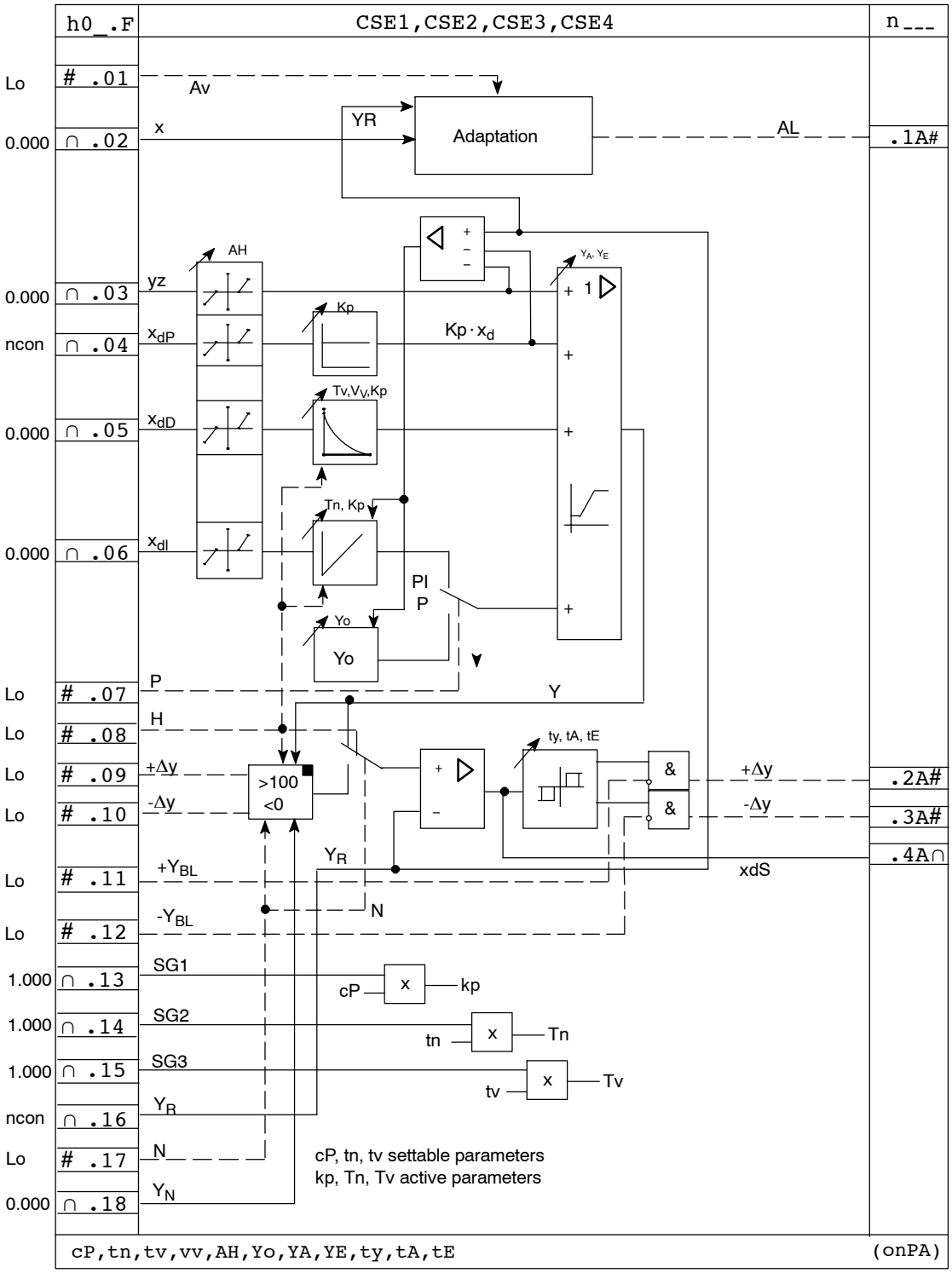


Figure 1–39 Arithmetic block h, S–controller with external position feedback

Note: The manipulated variable outputs +Δy and −Δy are permanently assigned to the digital outputs (see chapter 1.5.3, page 29).

- **Adaptation**

  The adaptation procedure represents a reliable and easy to operate commissioning tool. The adaptation procedure is far superior to manual optimization especially on slow controlled systems and in PID controller designs. It is activated by the operator and can be aborted at any time in the event of danger. The parameters determined by the adaptation can be changed and accepted specifically by the user. Unilinear controlled sistems can also be mastered in connection with the parameter control.
  In the parameterization mode AdAP which is only accessible in manual mode of the controller and AV input = High (adaptation preselection), the following presettings are made for the adaptation procedure:
  tU Monitoring time
  dPv Direction of step command
  dY Amplitude of step command
  tU is saved
  Restart batt no = oFF
  batt YES = previous value

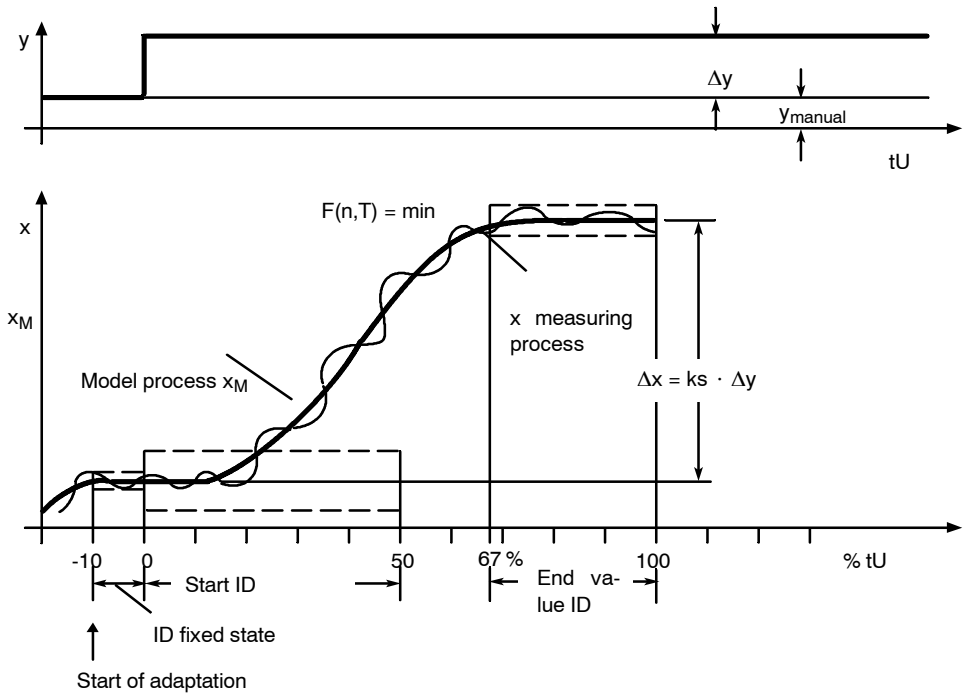


Figure 1–40 Time process of an adaptation without error messages in which tU = 2 x T95

The adaptation principle is divided into **line identification** and **controller design**.

- **Line identification**

  The controller is driven to the desired working point manually. By pressing the Enter key the set manual manipulated variable is changed by a step adjustable in the direction (dPv) and amplitude (dY). In K-controllers the y-step is output directly. The y-step is output at the end of 10 % of the set monitoring time (tU) if there was a fixed state of the

controlled variable during this time. Otherwise an error message is output with abortion of the identification (see chapter 3.3.2, Table 3-2, page 143).

The step response of the controlled system is then accepted with a max. 84 value pairs (time and amplitude). If the controlled variable x used for the adaptation is filtered (e.g. to suppress noise level), it should also be used for external formation of the control difference with the same time behavior; otherwise the adaptation could be faulty. The filters must be set accordingly in the adaptation. The measured values are read in with a scanning rate according to the cycle time. The storage procedure operates with cyclic data reduction and subsequent refilling so that slow controlled systems can be entered.

After the start identification has run, (the controlled variable x must have left the start identification band within 50 % of the set monitoring time tU), 95 % of the end value must be reached at $^2/_3$ of tU at the latest. The set monitoring time (tU) must be $\geq$ 2 T95 of the controlled system with safety reserve. The remaining time is required for the end value identification. The end value identification can also take place immediately after the start identification, but $^1/_3$ of the performed measurements are always required for the end value identification. Recording of the measured value pairs is ended on identifying the end value.

A comparison with the recorded transient function is now made based on the stored Ptn models with n = 1 to 8 and equal time constants T by variation of n and T. The determined line gain ks is transfered to the line models. The comparison is made over the minimum error area F (n, T).

Additionally a special entry of real dead times is made which then shifts the identified control line to higher orders.

Controlled lines with compensation and periodic transient of 1st to 8th order with a transient time T95 of 5 s to 12 h can be identified. Dead time parts are permissible. In S–controllers the transient time T95 should be twice the positioning time Ty.

Error checks are made during line identification in order to be able to prematurely abort the identification. There are 11 control steps altogether which are displayed by flashing on the digital x- and w- indicators when errors occur. As soon as an error message appears, the line identification is aborted and it must be restarted after correcting the presettings in the parameterization mode AdAP if necessary. Acknowledgement or listing of the error messages, see chapter 3.3.2, Table 3-2, page 143).

- **Controller design**

The controller is designed according to the method of amount optimum. This setting method is very robust and also allows variation of the line amplification. However, it generates an overshoot of approx. 5 % in the event of changes in the command variables.

The controller is designed for PI and PID behavior, therefore kp, tn and for PID tv are calculated, whereby the derivative gain is fixed at 5. The prerequisite for the effect of the differential part is that the D element is switched with xd. To determine the parameter Tv, tv must be $\neq$ oFF (onPA).

In S–controllers the response threshold AH is calculated in addition to kp, tn, tv. The parameters tA, tE and tY must be set according to the used actuating drives beforehand. If the transient time T95 is close to 2 tY (positioning time) overshoots may also be generated in controller designs with D-part.

In controlled systems of the 1st order a PI or PID controller design, in systems of the 2nd order a PID controller design cannot be implemented according to an amount optimum because in these cases kp goes to ∞. A controller design is produced in which the ratio of the line time constant to control loop constant is 6.

At the end of adaptation the previously active parameters (identification by .o) and the newly determined parameters (identification by .n) can be read in the parameterization mode AdAP. The new parameters for PI-controllers and for PID-controllers are offered.

In addition the determined line order 1 to 8 is displayed as a suffix to the Pi or Pid identification.
The selected parameters **.0, **.n Pi.* or **.n Pid.* (** = parameter name, * = line order 1 to 8) can be changed and accepted optionally.

The operating technique of the adaptation procedure is described in chapter 3.3.2.

- **Adaptation of the S–controller to the actuating drive**

  - **internal position feedback**

    The actuating time of the actuating drive is set with the online parameter tY
    (10 to 1000 s); the factory setting is 60 s.

    The online parameter tE should be selected at least great enough that the actuating drive starts moving reliably under consideration of the power switches connected before it. The greater the value of tE, the more resistant to wear and more gentle the switching and drive elements connected after the controller operate. Large values of tE require a greater dead band AH in which the controller cannot control defined because the resolution of the controlled variable diminishes with increasing turn–on duration.
    The factory setting is 180 ms for tE. This corresponds to a y resolution in a 60 s actuating drive of:

$$\Delta y = \frac{100\ \% \cdot tE}{tY} = \frac{100\ \% \cdot 180\ ms}{60\ s} = 0,3\ \%$$

    The minimum possible resolution is transposed with the line amplification Ks to the controlled variable:
    $\Delta x = K_s \cdot \Delta y$

    The parameter tA (minimum turn–off time) should be chosen at least great enough that the actuating drive is safely disconnected under consideration of the power switches connected before it before a new pulse appears (especially in the opposite direction). The greater the value of tA, the more resistant to wear the switching and drive elements connected after the controller operate and the greater the dead time of the controller under some circumstances. The value of tA is usually set identical to the value of tE.

    tA = tE = 120 to 240 ms are recommended for 60 s actuating drives. The more restless the controlled system, the greater the two parameters should be selected if this is reasonably justified by the controller result.

    The response threshold AH must be set according to the set tE and the resulting Δy or Δx. The condition

$$AH > \frac{\Delta x}{2} \text{ or } AH > \frac{K_s \cdot tE \cdot 100\ \%}{2 \cdot tY}$$

must be satisfied. Otherwise the controller outputs positioning increments although the control deviation has reached the smallest possible value due to the finite resolution. For setting AH, see section Response threshold AH.

- **external position feedback**

  The position control circuit is optimized with the online parameter tY. The same relationships apply as in the S–controller with internal position feedback whereby the dynamic of the position control circuit (non–linearities, follow–up) is added to the criteria of the processability of the positioning increments by the actuator. It will usually be necessary to select tY and the resulting response thresholds smaller than in the S–controller with internal position feedback for the above mentioned reasons.

  The position control circuit is optimized in the tracking mode, the manipulated variable changes are generated by switching over from manual to tracking mode. In addition connect the position increment outputs $\pm\Delta$y with L12, L13 for example and display YR and xdS on the displays. Occupy YN with a constant or freely switchable linear parameter depending on the desired optimization point, apply the control signal H to high and the control signal N to a key. Set approx. $\pm$5 % deviation from the tracking variable with the YR manipulated variable display in manual mode and then switch over to tracking mode. The position control circuit now runs to the set tracking variable. Observe the run–in on the xdS display or the Δy LEDs. During manual mode, the xdS display shows 0, during the tracking mode, the manual manipulated variable is tracked to the manipulated tracking variable so that a deviation needs to be set again for re–excitement in manual mode. In the case of unlinearity in the position control circuit, the optimization must take place in the range of greatest slope.

  - Set tA and tE so that the actuating drive can **just** process the positioning increments (see S–controller with internal feedback).
  - If filtering is provided: Set the filter of the y_R input to 0.01 Ty (real actuating time of the drive).
  - Increase tY until the position control circuit overshoots by switching over to the tracking mode (monitor counterpulse through the Δy-LEDs (e.g. L12, L13) in the xds display.
  - Reduce tY slightly again until the position control circuit is calm.

- **Automatic setting of the control parameters by the adaptation procedure**

  - **Preconditions for operating the adaptation:**

    A preparation input AV (h*.01) must be switched with a High signal at only one of the defined and positioned controllers. This defines the controller to be adapted.
    The x–input (h*.02) must be switched with the controlled variable. In S–controllers with external position feedback the fed back manipulated variable YR (h*.16) must be applied additionally to be able to enter the actuating value step. In S–controllers with internal position feedback the value of the step addition is determined from tY.

    The controller must be set to manual. The following parameters tU, dPv, dy must be set accordingly (see also chapter 3.3.2, page 138). The output AL (adaptation in progress) can be used to switch over displays to values of interest for example during adaptation. The data source AdAP can be switched in FCon for displaying the adaptation status, e.g. with L3.

- **tU: Monitoring time (parameterization mode AdAP)**

  tU is necessary for the error message only and has no influence on the identification quality. tU must be set at least double the transient time T_{95} of the controlled system. If you have little knowledge of the controlled system, use tU = oFF (factory setting) for adapting. After successful adaptation tU is automatically set to about $2T_{95}$. At tU $<$ 0.1 h (6 min), tU = oFF is displayed.

- **dPv: Direction of the step command (parameterization mode AdAP)**

  The direction of the controlled variable change from the set working point is selected with this configuring switch: $x_{Manual} \pm \Delta x = \pm ks$ ($y_{Manual} \pm \Delta y$). In controlled systems with batches it is recommendable to perform adaptation with increasing x and falling x. The averaged or dynamically more uncritical parameters can then be used for the control.

- **dy: Amplitude of the step command (parameterization mode AdAP)**

  The step command must be selected so great that the controlled variable changes by at least 5 % and the controlled variable change must be 5 times the average noise level. The greater the controlled variable change, the better the identification quality. Controlled variable changes of approx. 10 % are recommended.

- **Unilinear controlled systems**

  In unilinear controlled systems several adaptations should be made at different load states. The adaptation results and the controlling variable SG must be noted. The parameter sets determined in this way, related to the controlling variable SG, are then saved in a function transmitter FUL (arithmetic block c) and this can then be switched to the controlling input.
  In this way ideal controller results can be achieved even on unilinear controlled systems.

- **Notes on the adaptation results**

  D-part

  In S–controllers and K–controllers on controlled systems of 1st order the D-Part brings no noticeable advantages due to the finite positioning time Ty or for reasons founded in the control theory. The disadvantages in the form of wear on the positioning side carry greater weight.

  Range limits

  If one of the determined parameters reaches its range limits, the other parameter should be adjusted slightly in the opposite direction of action.
  If lines of the 8th order are identified, the determined Kp must be reduced for safety reasons. If the control loop is then too slow, the Kp must be increased again in the manual optimization.

  kp variation

  In the special case, controlled system of the 1st order in connection with PI and PID controllers and controlled systems of the 2nd order in connection with PID controllers, the kp can be varied freely. In controller design according to the amount optimum, Kp can be increased up to 30 % as a rule without the control behaviour becoming critical.

- **Manual setting of the control parameters without knowledge of the system behavior**

  The control parameters for optimum control of the system are not yet known in this case. To keep the control loop stable in any case, the following factory settings must be made (the values apply for both parameter sets):

Proportional action factor	Kp	=	0.1
Readjustment time	Tn	=	9984 s
Derivative action time	Tv	=	oFF

  - **P–controller (control signal P* = high)**
    - Set the desired setpoint and set the control difference to zero in manual mode.
    - The working point required for the control difference zero is set automatically at Yo = AUto (factory setting) in manual mode. The working point can also be entered manually by setting the online parameter Yo to the desired working point.
    - Switch to automatic mode.
    - Increase Kp slowly until the control loop tends to oscillate due to slight setpoint changes.
    - Reduce Kp slightly until the oscillations disappear.
  - **PD–controller (control signal P* = high)**
    - Set the desired setpoint and set the control difference to zero in manual mode.
    - The working point required for the control difference zero is set automatically at Yo = AUto (factory setting) in manual mode. The working point can also be entered manually by setting the online parameter Yo to the desired working point.
    - Switch to automatic mode.
    - Increase Kp slowly until the control loop tends to oscillate due to slight setpoint changes.
    - Switch Tv from oFF to 1 s.
    - Increase Tv until the oscillations disappear.
    - Increase Kp slowly until oscillations reappear.
    - Repeat the setting according to the two previous steps until the oscillations can no longer be eliminated.
    - Reduce Tv and Kp slightly until the oscillations are eliminated.
  - **Pi-controller (control signal P* = Low)**
    - Set the desired setpoint and set the control difference to zero in manual mode.
    - Switch to automatic mode.
    - Increase Kp slowly until the control loop tends to oscillate due to slight setpoint changes.
    - Reduce Kp slightly until the oscillations disappear.
    - Reduce Tn until the control loop tends to oscillate again.
    - Increase Tn slightly until the tendency to oscillate disappears.
  - **PiD-controller (control signal P* = Low)**
    - Set the desired setpoint and set the control difference to zero in manual mode.
    - Switch to automatic mode.
    - Increase Kp slowly until the control loop tends to oscillate due to slight setpoint changes.
    - Switch Tv from oFF) to 1 s.
    - Increase Tv until the oscillations disappear.
    - Increase Kp slowly again until the oscillations reappear.

- Repeat the setting according to the previous two steps until the oscillations cannot be eliminated again.
- Reduce Tv and Kp slightly until the oscillations stop.
- Reduce Tn until the control loop tends to oscillate again.
- Increase Tn slightly until the tendency to oscillate disappears.

- **Manual setting of the control parameters after the transient function**

  If the transient function of the controlled system is known or can be determined, the control parameters can be set according to the setting guidelines specified in the literature. The transient function can be recorded in the “Manual mode” position of the controller by a sudden change in the manipulated variable and the course of the controlled variable registered with a recorder. This will give a transient function similar to that shown in figure 1–41.

  Good average values from the setting data of several authors give the following rules of thumb:

  - **P–controller**

    Proportional action factor $Kp \approx \frac{Tg}{Tu \cdot Ks}$

  - **Pi-controller**

    Proportional action factor $Kp \approx 0,8 \cdot \frac{Tg}{Tu \cdot Ks}$

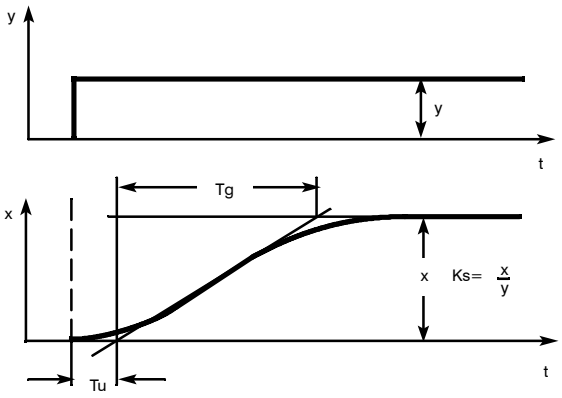
    Integral action time $Tn \approx 3 \cdot Tu$

  - **PiD controller**

    Proportional action factor $Kp \approx 1,2 \cdot \frac{Tg}{Tu \cdot Ks}$

    Integral action time $Tn \approx Tu$

    Derivativel action time $Tv \approx 0,4 \cdot Tu$



y	Manipulated variable
w	Command variable
x	Controlled variable
t	Time
Tu	Delay time
Tg	Compensation time
Ks	Transmission factor of the controlled system

Figure 1–41 Transient function of a controlled system with compensation

1.5.9 Restart Conditions

If the power supply fails, the analog and digital outputs become powerless, i.e. AA1 to AA3 : 0/4 mA. If AA4 is operated by the y–hold module, the output value depends on the power supply of the module (see chapter 1.4.2, page 12, **6DR2802-8A**)
BA1 to BA16 : Voltage output: Lo
BA9, 10 and 13, 14: Relay contact, changeover contact: rest position

Every power on triggers a further reset for the CPU.

The reset triggers a reset under the following conditions:

The restart conditions for counting, timing and memory functions are specified in the individual function blocks. The conditions depend on the configuring in mode hdEF (bAtt = YES, no). At batt = YES the last value before the power failure is usually used for starting, at batt = no the outputs of the function blocks are set specifically.

The non–storing functions react according to the available input data when restarting.

If special demands are made on the restart conditions, the conditions can be changed by connecting switch over functions with constants or parameters depending on the signals rES1, rES2.

1.5.10 Arithmetic

The analog variables are processed in a 3–byte floating point arithmetic. Two bytes are used for displaying the mantissa, 1 byte is reserved for the sign of mantissa and exponential and the exponential itself. This gives a decimal number range of -10^{19} to $+10^{19}$ with a resolution of 1 LSB = $1.6 \cdot 10^{-5}$ (16 bit resolution, LSB = least significant bit). The computing error per operation is a maximum 1 LSB on average.

The resolution is increased to 32 bits for some time–dependent functions (e.g. PID controller, integrators, clock) so that slow integration processes can also be shown as addition per computing cycle.

$$\frac{\Delta A}{\Delta t} = 2.4 \cdot 10^{-10} \cdot \frac{1}{t_c}$$

ΔA = value change at the output of a function block
t_c = cycle time

Process variables can be input and output through the analog inputs and outputs in the rated signal range from 0 % to +100 % (0/4 to 20 mA). The dynamic range ranges from –5 % to +105 %.

Process variable values of 0 to 100 % correspond to a number range of 0 to 1 in floating point arithmetic.

Computing operations are also performed with this number value. In additions and subtractions you can calculate in percent and in the area of floating point arithmetic:

100 % – 30 % + 20 % = 1 – 0.3 + 0.2 = 0.9 = 90 %

In multiplication, division, rooting and potency, calculation with the value 1 for 100 % is clearer.

Examples:

Muliplication

100 % · 100 % = 1 · 1 = 1 = 100 %
–70 % · 30 % = –0.7 · 0.3 = –0.21 = –21 %

Division

$$\frac{100\ \%}{100\ \%} = \frac{1}{1} = 100\ \%$$

$$\frac{-\ 80\ \%}{40\ \%} = \frac{-\ 0.8}{0.4} = -\ 2 = -\ 200\ \%$$

The following additional definitions
apply for division: 0/number = 0 ; ± number/0 → $\pm 10^{19}$; 0/0 = 0

Rooting

$$\sqrt{100\ \%} \mathrel{\hat{=}} \sqrt{1} = 1 \mathrel{\hat{=}} 100\ \%$$

$$\sqrt{64\ \%} \mathrel{\hat{=}} \sqrt{0,64} = 0,8 \mathrel{\hat{=}} 80\ \%$$

Only positive numbers may be rooted; the result is always set equal to zero when negative numbers are rooted.

Potency

$10^{100\ \%} \triangleq 10^{1} = 10 \triangleq 1000\ \%$
$10^{50\ \%} \triangleq 10^{0,5} = 3.162 \triangleq 316.2\ \%$
$10^{-50\ \%} \triangleq 10^{-0,5} = 0.316 \triangleq 31.6\ \%$

The private parameters are set in the dimensions %, s, 1 according to their function. The switchable parameters and the constants are set as a dimensionless number; their dimension and value depends on the function block with which they are connected.

1.6 Technical Data

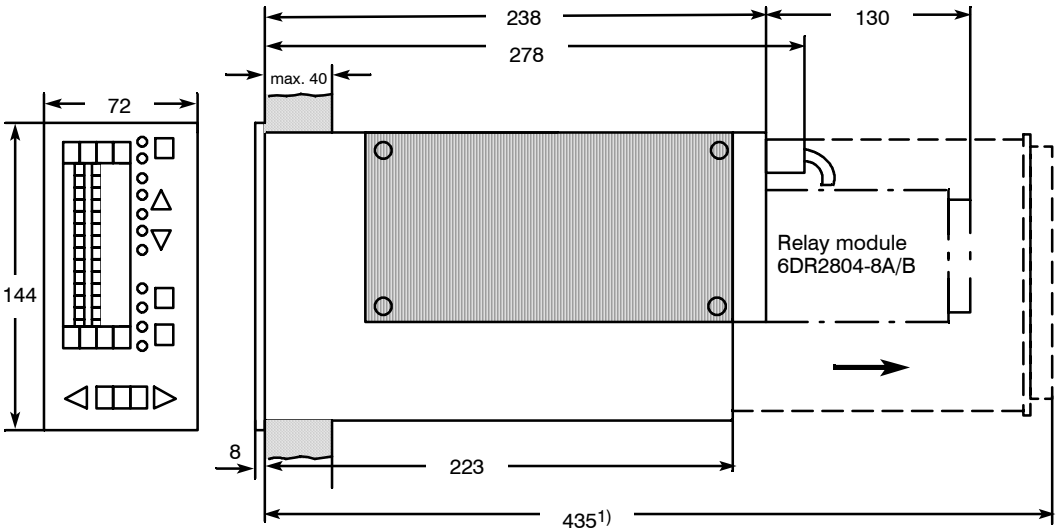
1.6.1 General Data

Installation position	any
Climate class according to IEC721	
Part 3-1 Storage 1k2	–25 to +75 °C
Part 3-2 Transport 2k2	–25 to +75 °C
Part 3-3 Operation 3k3	0 to +50 °C
Type of protection according to EN 60529	
Front	IP64
Housing	IP30
Connections	IP20

Controller design

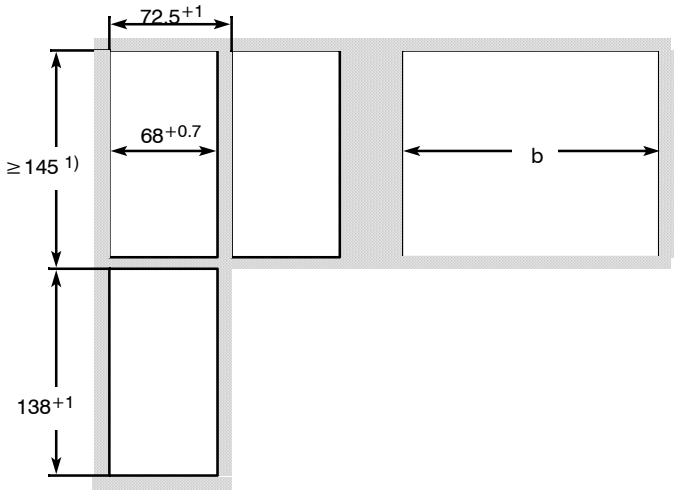
- Electrical safety
  - acc. to DIN EN 61 010 part 1,
  - Protection class I acc. to IEC 536
  - Safe disconnection between mains connection and field signals
  - Air and creep lines, unless specified otherwise, for overvoltage class III and degree of contamination 2
- EC declaration of conformity number 691.001
- CE mark conformity regarding:
  - EMC regulation 89/336/EWG and
  - LV regulation 73/23/EWG
- Spurious emission, interference immunity according to EN 61 326, NAMUR NE21 8/98

Weight, max. assembled	approx. 1.2 kg
Color	
Front module frame	RAL 7037
Front surface	RAL 7035
Material	
Housing, front frame	Polycarbonate, glass–fiber–reinforced
Front foil	Polyester
Rear panels, modules	Polybutylenterephthalate
Connection technique	
Power supply	
115/230 V AC	3–pin plug IEC320/V DIN 49457A
24 V UC	Special 2–pin plug
Field signals	plug–in terminals for 1.5 mm^2 AWG 14
Dimensions and panel cut–outs	see figure 1–42, page 94 and 1–43, page 94



1) Installation depth required to change the motherboard

Figure 1–42 Dimensions SIPART DR24, dimensions in mm



Number of controllers	Cut-out width b
2	140 +1
3	212 +1
4	284 +1
:	
:	
:	
10	716 +1

1) Installation close one above the other is allowed when the permissible ambient temperature is observed.

Figure 1–43 Panel cut–outs, dimensions in mm

1.6.2 Standard Controller

Power supply

Rated voltage	230 V AC switchable	115 V AC	24 V UC	
Operating voltage range	187 to 276 V AC	93 to 138 V AC	20 to 28 V AC	20 to 35 V DC[1)]
Frequency range	48 to 63 Hz			– – –
External current I_{Ext}[2)]	450 mA			
Power consumption				
Standard controller without options without I_{Ext} active power/apparent power (capacitive)	8 W/17 VA	8 W/13 VA	8 W/11 VA	8 W
Standard controller with options without I_{Ext} active power/apparent power (capacitive)	13 W/25 VA	13 W/20 VA	13 W/18 VA	13 W
Standard controller with options with I_{Ext} active power/apparent power (capacitive)	26 W/45 VA	26 W/36 VA	28 W/35 VA	28 W
Permissible voltage interruptions[3)]				
Standard controller without options without I_{Ext}	≤ 90 ms	≤ 70 ms	≤ 55 ms	≤ 30 ms
Standard controller with options without I_{Ext}	≤ 80 ms	≤ 60 ms	≤ 50 ms	≤ 25 ms
Standard controller with options with I_{Ext}	≤ 50 ms	≤ 35 ms	≤ 35 ms	≤ 20 ms

1) including harmonic
2) current transmitted from L+, BA, AA to external load
3) The load voltage of the AA is reduced hereby to 13 V, L+ to 15 V and the BA to 14 V

Table 1-3 Power supply standard controller

Analog inputs AE1 to AE3 and AE6 to AE11 (analog input module 3AE 6DR2800-8A)

Technical data under rated power supply conditions, +20 °C ambient temperature unless stated otherwise.

- **Voltage**

Rated signal range (0 to 100 %)	0/199.6 to 998 mV or 0/2 to 10 V shuntable
Dynamic range	≤ -4 to 105 %
Input resistance	
Difference	> 200 kΩ
Common mode	> 500 kΩ
Common mode voltage	0 to +10 V
Filter time constant	50 ms
Zero point error	0.1 % + AD converter error
End value error	0.2 % + AD converter error

Linearity error	see AD converter
Common mode error	0.07 %/V
Temperature influence	
Zero point	0.05 %/10 K
End value	0.1 %/10 K
Static destruction limit	± 35 V

- **Current**

Rated signal range	0/4 to 20 mA
Dynamic range	–1 to 21 mA
Input resistance	
Difference (load)	49.9 Ω ± 0.1 %
Common mode	> 500 kΩ
Common mode voltage	0 to +10 V
Filter time constant	50 ms
Zero point error	see AD converter
End value error	see AD converter
Linearity error	see AD converter
Common mode error	0.07 %/V
Temperature influence	
Zero point	0.05 %/10 K
End value	0.1 %/10 K

Analog outputs AA1 to AA3

Rated signal range (0 to 100 %)	0 to 20 mA or 4 to 20 mA
Dynamic range	0 to 20.5 mA or 3.8 to 20.5 mA
Load voltage	from –1 to 18 V
No load voltage	≤ 26 V
inductive load	≤ 0.1 H
Filter time constant	300 ms
Residual ripple 900 Hz	≤ 0.2 %
Resolution	11 bits
Load dependence	≤ 0.1 %
Zero point error	≤ 0.3 %
End value error	≤ 0.3 %
Linearity	≤ 0.05 %
Temperature influence	
Zero point	≤ 0.1 %/10 K
End value	≤ 0.1 %/10 K
Static destruction limit	–1 to 35 V

Measuring transducer feed L+

Rated voltage	+20 to 26 V
Load current	≤ 100 mA, short–circuit–proof
Short–circuit current	≤ 20 mA clocking
Static destruction limit	–1 to +35 V

Digital inputs BE1 to BE4

Signal status 0	≤ 4.5 V or open
Signal status 1	≥ 13 V
Input resistance	≥ 27 kΩ
Static destruction limit	± 35 V

Digital outputs BA1 to BA8 (with wired or diodes)

Signal status 0	≥ 13 V
Signal status 1	+19 to 26 V
Load current	≤ 50 mA
Short–circuit current	≤ 80 mA clocking
Static destruction limit	–1 to +35 V

Cycle time

Variable min 60 ms	+ 2 ms per basic function + 5 ms per complex function

A/D conversion

Procedure	successive approximation per input >120 conversions and averaging within 20 or 16.67 ms
Resolution	11 bits ≙ 0.06%
Dynamic range	–5 to 105%
Zero point error	≤ 0.2 %
End value error	≤ 0.2 %
Linearity error	≤ 0.2 %
Temperature influence	
Zero point	≤ 0.05 %/10 K
End value	≤ 0.1 %/10 K

D/A conversion see AA1 to AA3

Parameters

Setting	with tA2/3 (more – less)
Speed	progressive
Accuracy	
Time parameters	typical: ±0.1 % ≤ ±0.5 % over the whole temperature range
all others	according to resolution, absolute

Display technique

- Digital displays dd1, dd2	$4^1/_2$digit 7-segment LED
Color	
dd1	green
dd2	red
Digital height	7 mm
Display range	start–end adjustable
Number range	–1999 to 19999
Overflow	< –1999: –oFL
	> 19999: oFL
Decimal point	adjustable (fixed point) _.___ to _ _ _ _
Repetition rate	adjustable 1 to 100 cycles/display
Resolution	1 digit, but not better than AD converter
Display error	according to AD converter and analog inputs
- Digital displays dd3	3digit 7-segment LED
Color	yellow
Digital height	7 mm
Display range	start–end adjustable
Number range	–199 to 999
Overflow	< –199: oFL
	> 999: oFL
Decimal point	adjustable (fixed .) _ _.– to _ _ _
Repetition rate	adjustable 1 to 100 cycles/display
Resolution	1 digit, but not better than AD converter
Display error	according to AD converter and analog inputs
- Analog display dA1, dA2	
Color dA1	red
dA2	green
Display range	LED array with 30 LEDs
Signal range	adjustable, from –199.9 % to +199.9 %
Overflow	<–0.85 % of the display range 1st LED flashes
	>100.85 % of the display range 30th LED flashes
Resolution	1.7 % of the display range, by alternating lighting of 1 or 2 LEDs, the center point of the field of light serves as a pointer
Repetition rate	cyclic

1.6.3 Technical Data of the Options Modules

6DR2800-8A 3AE I/U module Analog inputs AE6 to AE8 (slot 6), AE9 to AE11 (slot 5), see chapter 1.6.2, page 95, AE1 to AE3

6DR2800-8J/R Analog inputs AE4 (slot 2), AE5 (slot 3)

Signal transformer for **Order number:**	**1AE** **Current** **6DR2800-8J**	**1AE** **Voltage** **6DR2800-8J**	**1AE** **Resistance potentiometer** **6DR2800-8R**
Range start	0 or 4 mA [1]	0 V or 2 V[1] or 199.6 mV [1]	0 Ω
Min. span (100 %)			ΔR ≥ 0.3 R [3]
Max. zero point suppression			RA ≤ 0.2 R [3]
Range end	20 mA	10 V, 998 mV	RA + 1.1 R [3]
Dynamic range	–5 to 105 %	–5 to 105 %	–5 to 105 %
Input resistance			
Difference	49.9 Ω ±0,1 %	200 kΩ	
Common mode	500 kΩ	≥ 200 kΩ	
Permissible common mode voltage	0 to +10 V	0 to +10 V	
Supply current			5 mA ±5%
Line resistance			
Two–wire circuit			–
Three–wire circuit			per < 10 Ω
Four–wire circuit			–
Filter time constant ±20 %	50 ms	50 ms	50 ms
Error [2]			
Zero point	≤ 0.3 %	≤ 0.2 %	≤ 0.2 %
Gain	≤ 0.5 %	≤ 0.2 %	≤ 0.2 %
Linearity	≤ 0.05 %	≤ 0.05 %	≤ 0.2 %
Common mode	≤ 0.07 %/V	≤ 0.02 %/V	–
Influence of temperature [2]			
Zero point	≤ 0.05 %/10 K	≤ 0.02 %/10 K	≤ 0.1 %/10 K
Gain	≤ 0.1 %/10 K	≤ 0.1 %/10 K	≤ 0.03 %/10 K
Stat. destruction limit			
between the inputs referenced to ground	±40 mA ±35 V	±35 V ±35 V	±35 V ±35 V

1) Measuring start by configuring
2) Without errors of the A converter
3) with R = RA +Δ R + RE adjustable in three ranges:
R = 200 Ω, R = 500 Ω, R = 1000 Ω

Table 1-4 Technical data for I/U module 6DR2800–8J/R

6DR2800-8V UNI module Analog inputs AE4 (slot 2), AE5 (slot 3)

Analog inputs AE4, AE5 Slot 2, 3	**mV** [1]	**TC** [2] °C	**Pt100**	**R** R ≤ 600 Ω	**R** R ≤ 2,8 kΩ
Range start MA	≥ -175 mV	≥ -175 mV	≥ -200 °C	≥ 0 Ω	≥ 0 Ω
Range end ME	≤ +175 mV	≤ +175 mV	≤ +850 °C	≤ 600 Ω	≤ 2,8 kΩ
Span Δ = ME - MA	parameterizable 0 to Δmax				
Min. recommended span	5 mV	5 mV	10 K	30 Ω	70 Ω
Measuring transducer fault message MUF	-2.5 % ≥ MUF ≥ 106.25 % [3]				
Input current	≤ 1 μA	≤ 1 μA	–	–	–
Supply current	–	–	400 μA	400 μA	140 μA
Potential isolation					
Test voltage	500 V AC				
Perm. common mode voltage	≤ 50 V UC	≤ 50 V UC	–	–	–
Line resistance					
2L RL1+RL4	≤ 1 kΩ	≤ 300 Ω	≤ 50 Ω		
3L: (RL1) = RL2 = RL4	–	–	≤ 50 Ω		
4L: RL1 to RL4	–	–	≤ 100 Ω		
Break signaling	without	≥ 500 to 550 Ω	all terminals	Break between terminal 2–3	
Error					
Transmission	± 10 μV	± 10 μV	± 0.2 K	± 60 mΩ	± 200 mΩ
Linearity	± 10 μV	± 10 μV	± 0.2 K	± 60 mΩ	± 200 mΩ
Resolution/noise	± 5 μV	± 2 μV	± 0.1 K	± 30 mΩ	± 70 mΩ
Common mode	± 1 μV/10 V	± 1 μV/10 V			
Internal reference point	–	± 0.5 K	–	–	–
Temperature error					
Transmission	± 0.05 %/10 K [3]				
Internal reference point	–	± 0.1 K/10 K			
Statistical destruction limit	± 35 V	± 35 V	–	–	–
Cycle time	100 ms	200 ms	300 ms	200 ms	200 ms
Filter constant adaptive	<1.5 s	<2 s	<2 s	<1.5 s	<1.5 s

1) 20 mA, 10 V with measuring range plug 6DR2805-8J
2) Types see CAE menu, internal reference point (pluggable terminal block) 6DR2805-8A
3) Referenced to parameterizable span D = ME - MA

Table 1-5 Technical data for UNI module 6DR2800–8V

6DR2805-8J Measuring range plug 20 mA/10 V

- **20 mA**

Conversion to 100 mV	±0.3 %
Load terminal 1 - 2	50 Ω
1 - 3	250 Ω
Stat. destruction limit	±40 mA

- **10 V**

Divider to 100 mV	±0.2 %
Input resistance	90 k
Stat. destruction limit	±100 V

6DR2801-8D 2BA Relay 35 V+ Digital outputs BA9 and BA10 (slot 5) or BA13 and BA14 (slot 6)

- **Contact material** Ag/Ni

- **Contact load capacity**

Switching voltage	
AC	≤ 35 V
DC	≤ 35 V
Switching current	
AC	≤ 5 A
DC	≤ 5 A
Rating	
AC	≤ 150 VA
DC	≤100 W for 24 V
	≤ 80 W for 35 V

- **Service life**

mechanical	$2x10^7$ Switching processes
electrical	
24 V/4 A ohmic	$2x10^6$ Switching processes
24 V/1 A inductive	$2x10^5$ Switching processes

- **Spark quenching element**

Series circuit	1 μF/22 Ω parallel to it varistor 75 Vrms

6DR2801-8E 4BA 24 V + 2BE Digital outputs BA9 to BA12 and digital inputs BE5 and BE6 (slot 5) or
digital outputs BA13 to BA16 and digital inputs BE10 and BE11 (slot 6)

- **Digital outputs**

Signal status 0	≤ 1.5 V or open, residual current ≤ 50 μA
Signal status 1	+19 to 26 V
Load current	≤ 30 mA
Short–circuit current	≤ 50 mA clocking
Static destruction limit	–1 V to +35 V

- **Digital inputs**

Signal status 0	≤ 4.5 V or open
Signal status 1	≥ 13 V
Input resistance	≥ 2.4 kΩ
Static destruction limit	±35 V

6DR2801–8C 5BE 24 V Digital inputs BE5 to BE9 (slot 5), BE10 to BE14 (slot 6)

Signal status 0	≤ 4.5 V or open
Signal status 1	≥ 13 V
Input resistance	≥27 kΩ
Staistical destruction limit	±35 V

6DR2802-8A 1AA(y_{hold}) Analog outputs AA4 (slot 6), AA7 (slot 5)

- **Analog output AA4/AA7**

Rated signal range (0 to 100 %)	0 to 20 mA or 4 to 20 mA
Dynamic range	0 to 20.5 mA or 3.8 to 20.5 mA
Load voltage	
for supply	
from controller	–1 to 18 V
by U_H > 22.5 V	–1 to 15 V
by U_H = 20 V	–1 to 12.5 V
No load voltage	≤ 26 V
Inductive load	≤ 0.1 H
Time constant	300 ms
Residual ripple 900 Hz	≤ 0.2 %
Resolution	0.1 %
Load dependence	≤ 0.1 %
Zero point error	≤ 0.2%
End value error	≤ 0.1 %
Linearity	≤ 0.05 %
Temperature influence	
Zero point	≤ 0.1 %/10 k
End value	≤ 0.1 %/10 k
Static destruction limit	–1 V to +35 V

- **Digital output $\overline{St}$**

Signal status 0	≤ 1.5 V
Signal status 1	+19 to 26 V
Load current	≤ 30 mA, short–circuit–proof
Short–circuit current	≤50 mA clocking
Static destruction limit	–1 to +35 V

- **Auxiliary voltage U_H**

Voltage range	+20 to +30 V (including harmonic)
Current consumption	
with supply from controller	≤ 6 mA
with supply by U_H	≤ 70 mA
Static destruction limit	±35 V

6DR2802–8B 3AA and 3BE Analog outputs AA7 to AA9, digital inputs BE5 to BE7 (slot 5);
Analog outputs AA4 to AA6 (slot 6), digital inputs BE10 to BE12 (slot 5);

- **Analog outputs**

Rated signal range (0 to 100 %)	0 to 20 mA or 4 mA to 20 mA
Dynamic range	0 to 20.5 mA or 3.8 mA to 20.5 mA
Load range	from –1 V to 18 V
No load voltage	≤ 26 V
Inductive load	≤ 0.1 H
Time constant	10 ms
Residual ripple 900 Hz	≤ 0.2 %
Resolution	10 bits
Load dependence	≤ 0.1 %
Zero point error	≤ 0.3 %
End value error	≤ 0.3 %
Linearity	≤ 0.05 %
Temperature influence	
Zero point	≤ 0.1 %/10 K
End value	≤ 0.1 %/10 K
Static destruction limit	–1 V to 35 V

- **Digital inputs**

Signal status 0	≤ 4.5 V or open
Signal status 1	≥ 13 V
Input resistance	≥ 27 kΩ
Static destruction limit	± 35 V

6DR2803-8P PROFIBUS–DP

Transmittable signals	RS 485, PROFIBUS-DP protocol
Transmittable data	Operating state, process variables, parameters and configuring switches
Transmission procedure	
PROFIBUS-/DP protocol	According to DIN 19245, part 1 and part 3 (EN 50170)
Transmission speed	9.6 kBit/s to 1.5 MBit/s
Station number	0 to 125
Time monitor of the data communication	Can be configuring on the controller in connection with the DP–watchdog
Electrical isolation between	
Rxd/Txd-P/-N and the controller	50 V UC common mode voltage
Test voltage	500 V AC
Repeater control signal CNTR-P	TTL level with 1 TTL load
Power supply VP (5 V)	5 V -0.4 V/+0.2 V; short–circuit proof
Line lengths; per segment at 1.5 MBit/s	200 m; see ET200 6ES5 998-3ES12 manual for further data

6DR2803-8C Serial interface

Transmittable signals	RS 232, RS 485 or SIPART BUS *) shuntable
Transmittable data	Operating state, process variables, parameters and configuring switches
Transmission procedure	According to DIN 66258 A or B
Character format	10 bits (Start bit, ASCII characters with 7 bits, Parity bit and Stop bit)
Hamming distance h	2 or 4
Transmission speed	300 to 9600 bit/s
Transmission	Asynchronous, semi–duplex
Addressable stations	32
Time monitoring of the data communication	1 s to 25 s or without
Electrical isolation between Rxd/Txd and the controller	
Max. common mode voltage	50 V UC
Test voltage	500 V AC

	RS 232	RS 485
Receiver input Rxd Signal level 0 Signal level 1 [1] Input resistance	 0 to +12 V [2] –3 to –12 V [2] 13 kΩ	 $U_A > U_B$, +0.2 to +12 V $U_A < U_B$, -0.2 to -12 V 12Ω
Send output Txd Signal level 0 Signal level 1 [1]	 +5 to +10 V –5 to –10 V	 $U_A > U_B$, +1.5 to +6 V $U_A < U_B$, -1.5 to -6 V
Load resistance	≤ 1.67 mA	54Ω

1) Signal status 1 is the rest state
2) Input protected with 14 V Z-diode, greater voltages possible with current limiting to 50 mA.

Line capacitance or lengths
at 9600 bits/s

	Power capacitance	Reference values line lengths	
		Ribbon cable without shield	Round cable with shield
RS232 end–to–end	≤ 2.5 nF	50 m	25 m
RS 485 bus	≤ 250 nF	1000 m	1000 m

*) SIPART bus operation is no longer possible! The bus driver is no longer available!

6DR2804-8A/B Coupling relay 230 V

1 relay module	6DR2804-8B
2 relay modules	6DR2804-8A
per relay module	2 relays with 1 changeover contact each with spark quenching element
- **Contact material**	Silver-cadmium oxide
- **Contact load capacity**	
Switching voltage	
AC	≤ 250 V
DC	≤ 250 V
Switching current	
AC	≤ 8 A
DC	≤ 8 A
Rating	
AC	≤ 1250 VA
DC	≤ 30 W at 250 V ≤ 100 W at 24 V
- **Service life**	
mechanical	$2x10^7$ Switching processes
electrical AC 230 V, ohmic	$2x10^6/I(A)$ switching processes
- **Spark quenching element**	Series circuit 33 nF/220 Ω parallel to it Varistor 420 V_{rms}
- **Exciter winding**	
Voltage	+19 at +30 V
Resistor	1.2 kΩ ± 180 Ω
- **Electrical isolation between**	
Exciter winding – Contacts Air and relay module – relay module (6DR2804-8A)	Safe isolation [1] by increased insulation, air and creep lines for overvoltage class III and degree of contamination 2
Contact – Contact of a relay module	Safe isolation [1] by increased insulation, air and creep lines for overvoltage class II and degree of contamination 2
- **Type of protection**	
Housing	IP50 according to DIN 40050
Connections (in plugged status)	IP20 according to DIN 40050
- **Housing material**	polyamide 66
- **Mounting rail assembly** on	NS35/7.5 DIN EN 5002 NS35/15 DIN EN 50035 NS32 DIN EN 50035
- **Dimensioned drawing**	see figure 1–44, page 106

[1] according to DIN EN 61010 Part 1

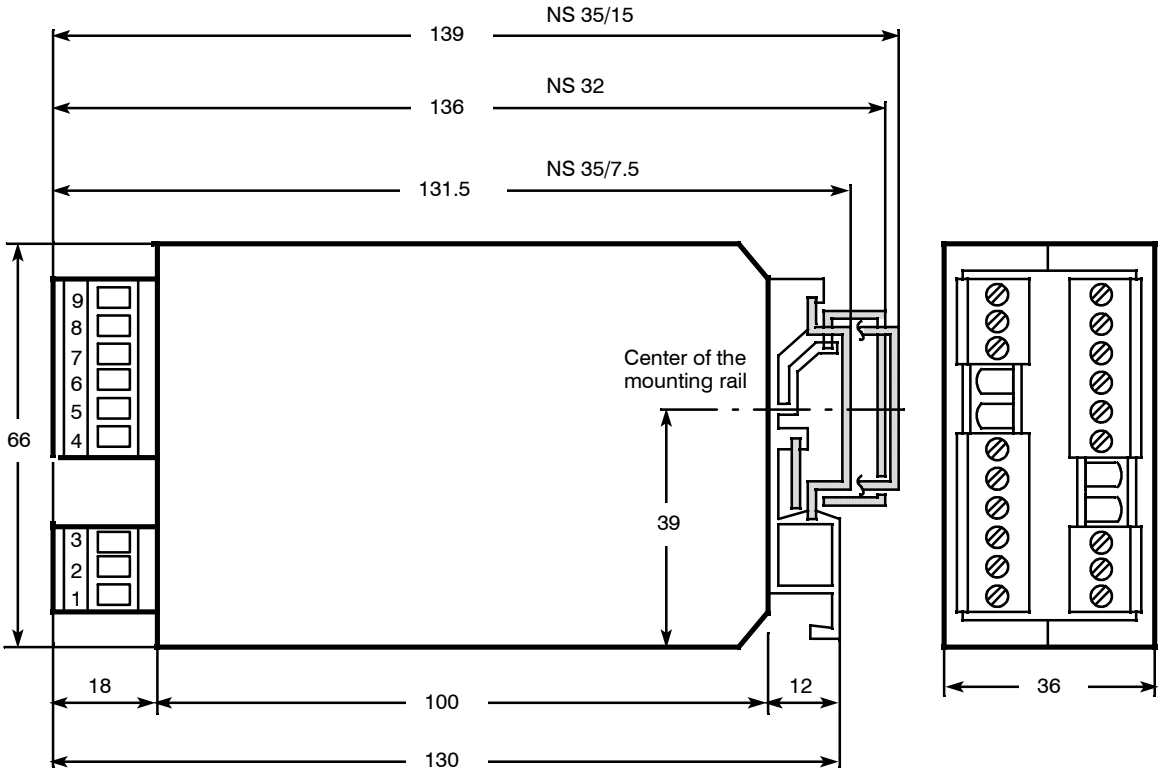


Figure 1–44 Dimensioned diagram coupling relay, dimensions in mm

2 Installation

2.1 Mechanical Installation

- **Selecting the Installation Site**

  Maintain an ambient temperature of 0 to 50 °C. Don't forget to allow for other heat sources in the vicinity. Remember that if instruments are stacked on top of each other with little or no gap between them, additional heat will be generated. Front and rear sides of the controller must be easily accessible.

- **Panel mounting**

  The SIPART DR24 is installed either in single panel cut–outs or in open tiers (see figure 1–42, page 94 and 1–43, page 94 for dimensioned drawing).

  - The upper edge of the panel cut–out must be left unpainted to ensure good interference suppression of the controller even at high frequencies. A good HF ground connection is established by the contact spring protruding from the top of the SIPART DR24.
  - If necessary: Slide the self–adhesive gasket ring for sealing the front frame/front panel over the body and adhere onto the reck of the body (see chapter 5.2, page 173, item 2.6).
  - Insert SIPART DR24 into the panel cut–out or open tier from the front and fit the two clamps provided to the controller unit from the rear so that they snap into the cut–outs in the housing.
  - Align SIPART DR24 and do not tighten the locking screws too tight. The tightening range is 0 to 40 mm.

2.2 Electrical Connection

The layout of the connecting elements is shown in figure 2-1, page 109.

WARNING

The "Regulations for the installation of power systems with rated voltages under 1000 V" (VDE 0100) must be observed in the electrical installation!

- **PE conductor connection**

  Connect the PE conductor to the ground screw (see figure 2-1, page 109) on the back of the controller. When connecting to 115 or 230 V AC mains supply, the PE conductor can also be connected through the three–pin plug (see figure 2-1, page 109). The controller's ground connection may also be connected with the PE conductor (grounded extra low voltages).

WARNING

Disconnection of the PE conductor while the controller is powered up can make the controller potentially dangerous. Disconnection of the PE conductor is prohibited.

- **Power supply connection**

The power supply is connected on 115 V or 230 V AC systems by a three–pin plug IEC 320/V DIN 49457 A , on 24 V UC systems by a special 2–pin plug (polarity irrelevant). The plugs are supplied with the unit.

WARNING

Set the mains voltage selection switch (see figure 2-1, page 109) in the no–voltage state to the existing mains voltage.
It is essential to observe the mains voltage specified on the rating plate or on the mains voltage switch (115/230 V AC) or on the voltage plate (24 V DC)!
Feed the power cables via a circuit breaker within easy reach (fire safety according to IEC 66E (sec) 22/DIN VDE 0411 Part 100). When connected to an unprotected power supply, the controller must be supplied via a circuit breaker. The circuit breaker is not required if one already exists ($\leq$ 30 Vrms or $\leq$ 42,4 V DC and current $\leq$ 8 A or source under all load conditions $\leq$ 150 VA or fuse element which responds at $\leq$ 150VA).
The circuit breaker can be omitted if the 24 V UC power supply unit is protected by $\leq$ 4 A (35 V DC) (slow-blow 3.15 A is required at least).

- **Connection of measuring and signal lines**

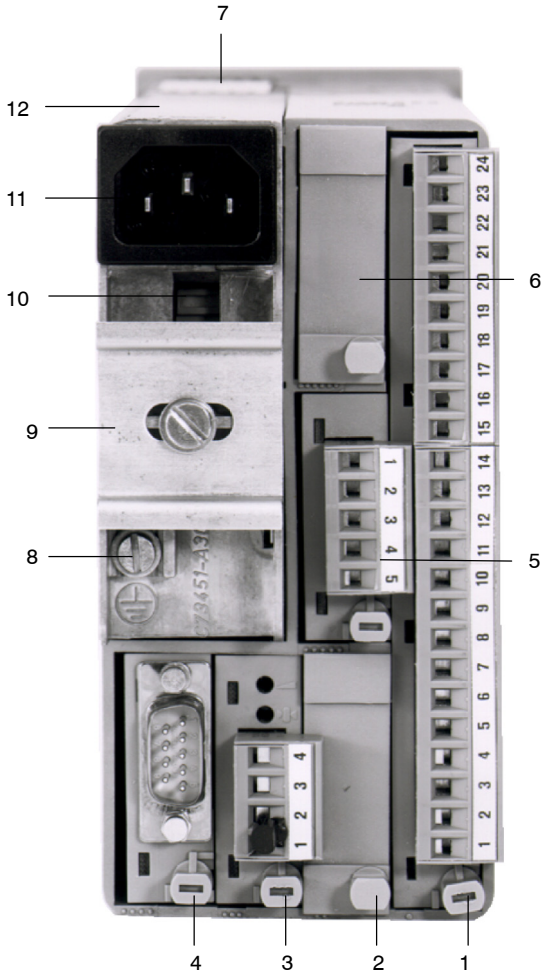
The process signals are connected via plug–in terminal blocks that can accommodate cables of up to 1.5 mm^2 (AWG 14) cross–section.

Standard controller	Slot 1	14 and 10–pin
Option modules	Slots 2 and 3	4–pin
	Slot 5 and 6	5 and 6–pin
Interface relays	“Slots” 7 and 8	3 and 6–pin

The slots 1 to 8 must be marked in the circuit diagrams and at the terminal blocks.

Signal lines should be laid separately from power cables to avoid the risk of interference couplings. If this is not possible, or – due to the type of installation – the controller may not function properly as a result of interference on the signal lines, the signal lines must be screened. The screen must be connected to the PE conductor of the controller or one of the ground connections, depending on the fault source’s reference point. The screen should always only be connected to one side of the controller when it is connected to the PE conductor to prevent creation of a ground loop.

The SIPART DR24 is designed with a high electromagnetic compatibility (EMC) and has a high resistance to HF interference. In order to maintain this high operational reliability we recommend that all inductances (e.g. relays, contactors, motors) installed in the vicinity of or connected to the controllers should be assembled with suitable suppressors (e.g. RC combinations)!



1 Slot 1
Main board
AE1 to AE3 (I/U)
AA1 to AA3
BE1 to BE4
BA1 to BA8 24 V
L+, M

2 Slot 2
AE4 (I/U, R, P, T, V)

3 Slot 3
AE5 (I/U, R, P, T,V)

4 Slot 4
Serial interface

5 Slot 5

4BA 24 V+2BE	BA9 to BA12, BE5 to BE6
2BA relay	BA9, BA 10
5BE	BE5 to BE9
1AA	AA7
3AE	AE9 to AE11
3AA+3BA	AA7 to AA9, BE5 to BE7

6 Slot 6

4BA 24 V+2BE	BA13 to BA16, BE10 to BE11
2BA relay	BA13, BA14
5BE	BE10 to BE14
1AA(y-hold)	AA4
3AE	AE6 to AE8
3AA+3BE	AA4 to AA6, BE10 to BE12

7 PE conductor contact spring

8 Grounding screw

9 Mounting rail
(included in the scope of supply of the 6DR2 804-8A/B relay modules)

10 Mains voltage selection switch

11 Mains plug

12 Power supply unit

Figure 2-1 Rear panel

- **Connection of the serial interface**

  For V.28 point–to–point connections of the SES, a 9–pin socket strip for round cables in solder technique is available.

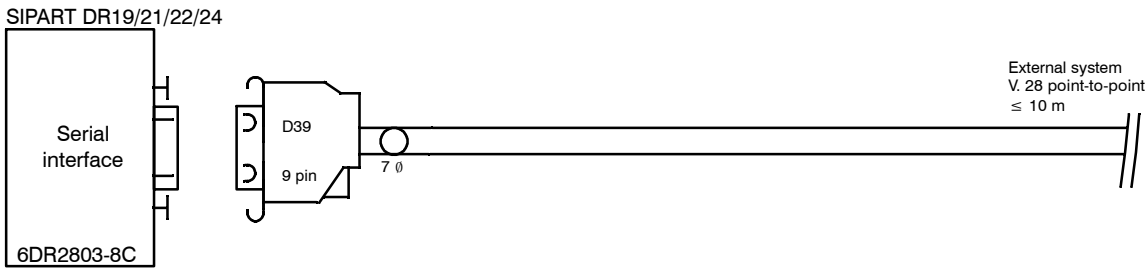


Figure 2-2 Connector plug serial interface

9–pin D–plug for round cables (screw terminal	C73451-A347-D39
Recommended cable: 4–core unscreened round cable	JE-LiYY 4x1x0.5 BdSi

- **Zero volt system**

  The SIPART DR24 controllers only have a 0V conductor (ground, GND) on the process side which is output double at terminals 1/1 and 1/2 of the standard controller. If these GND connections are not sufficient, additional proprietary terminals can be snapped onto the DIN rail on the power pack. The controller uses a common reference for both inputs and outputs, all process signals are referred to this point.
  The reference line is also connected to vacant module terminals. These may only be used if practically no input current flows through this connection (see for example figure 2-14, page 116, I 4L).

  The power supply connection is electrically isolated from the process signals. In systems with unmeshed control circuits, the controllers need not be interconnected. In meshed control loops the GND connections of all controllers must be fed singly to a common termination or the continuous GND rail with a large cross-section. This common termination may be connected with the system's PE conductor at one point.

  Since only currents 0/4 to 20 mA are used in analog signal exchange between the units and these are interpreted as a four–pole measurement (differential amplifier with electronic potential isolation), voltage dips on ground are not interpreted as errors (see figures 2-27, page 124 to 2-33, page 126).

  The signal–to–noise ratio on digital signals is so great that voltage dips on the GND rail can be ignored.

2.2.1 Block Diagram

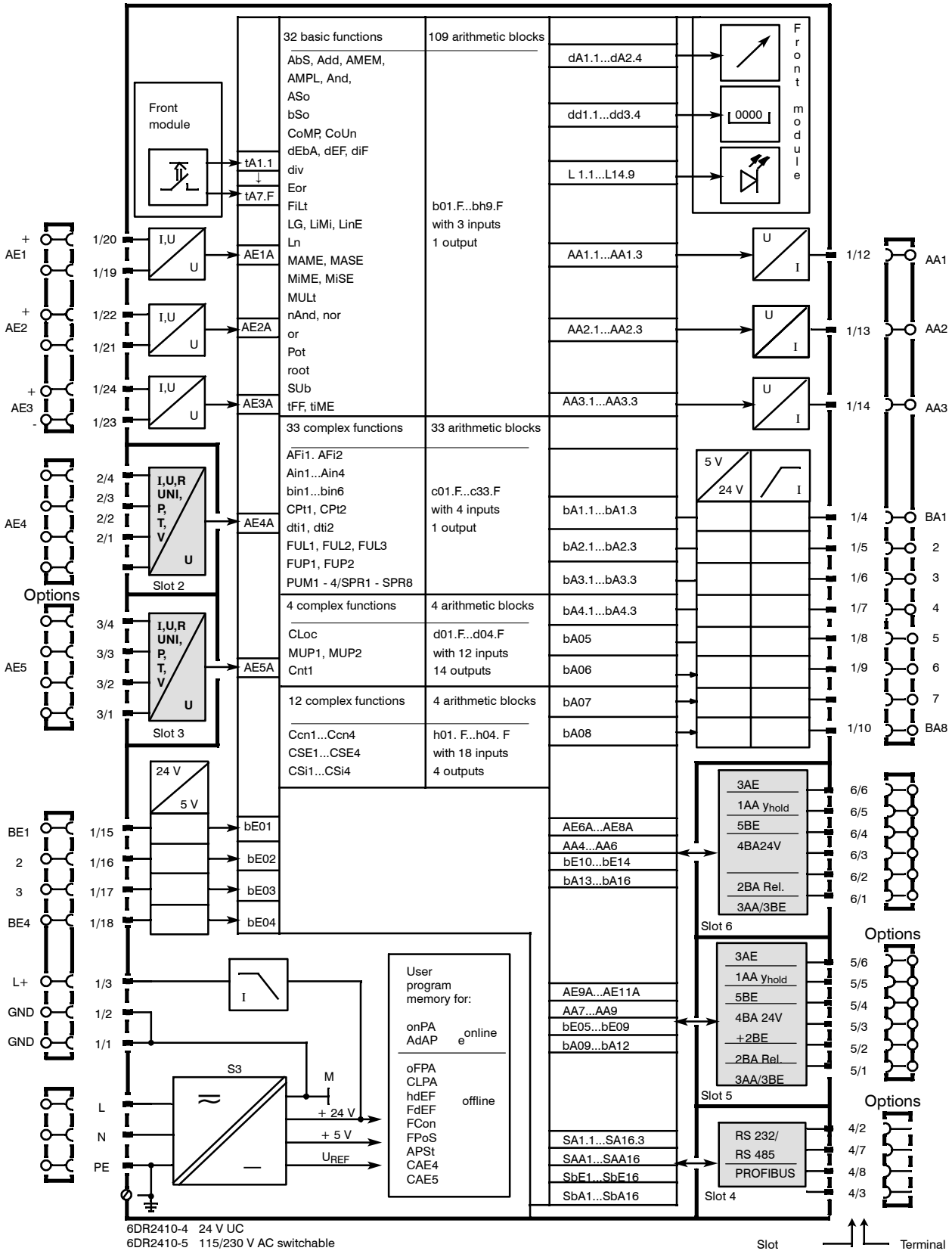


Figure 2-3 Block diagram SIPART DR24

2.2.2 Wiring of the standard Controller

- **Power supply connection**

  Attention:
  Set mains voltage selection switch (see fig. 2-1, page 109) in no–voltage state according to the available mains voltage!

  - 6DR2410-5 115/230 V AC, switchable

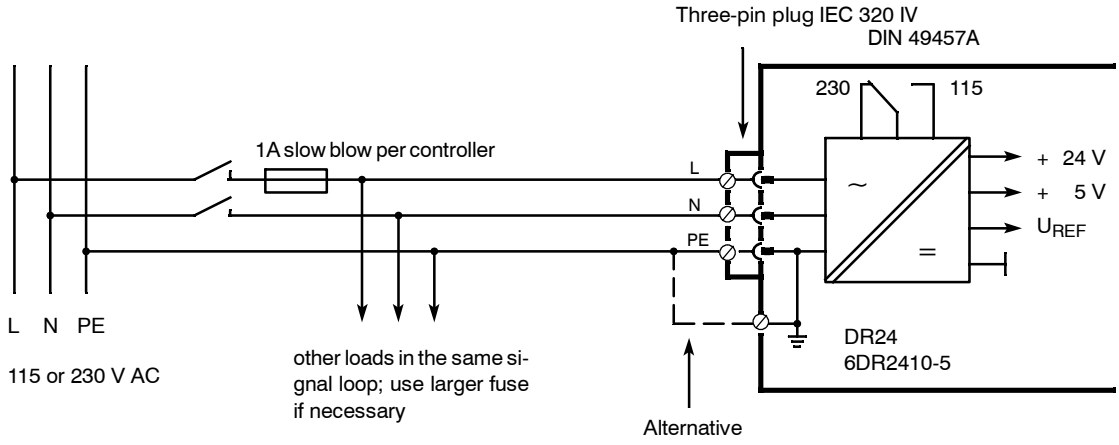


Figure 2-4 Wiring diagram of power supply 115/230 V AC

  - 6DR2410-4 24V UC

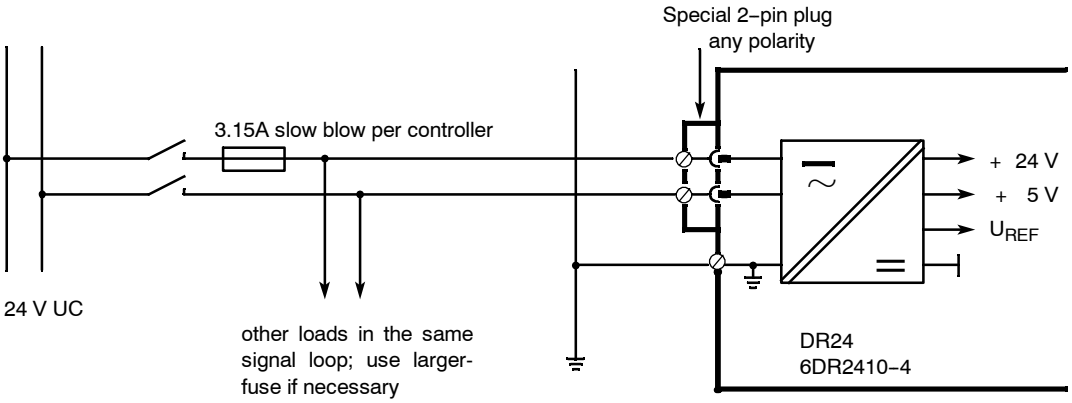
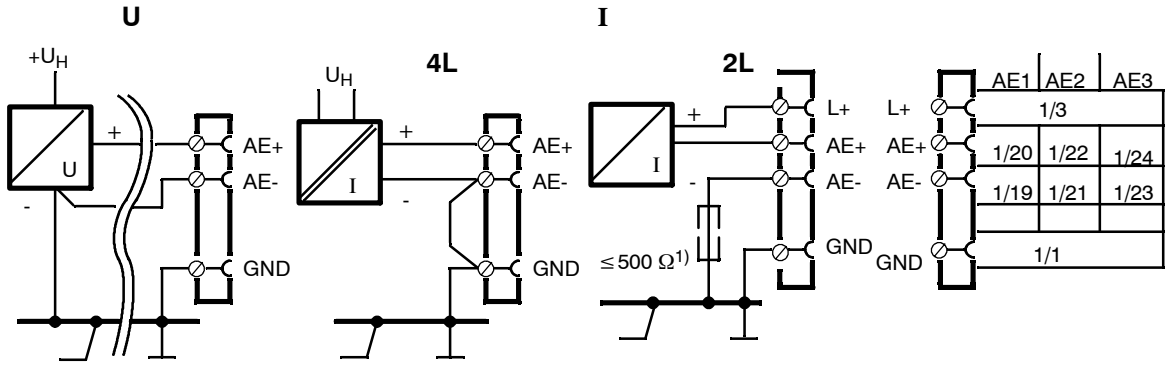


Figure 2-5 Wiring diagram of power supply 24 V DC

- **AE1 to AE3**

  - **Wiring**



See chapter 2.2.4, page 123 for alternative wiring

Set AE 1 to AE 3 to 0 or 4 mA in hdEF

1) potential load impedance from additional instruments

Figure 2-6 AE1 to AE3 U or I wiring diagram

  - **Jumper settings**

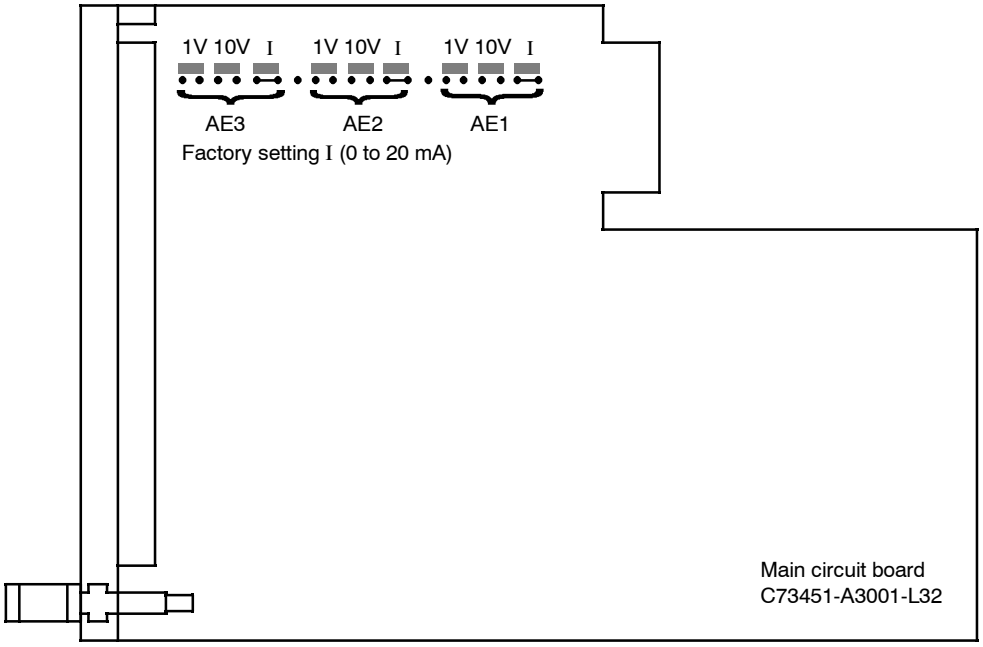


Figure 2-7 Jumper settings AE1 to AE3

- **BE1 to BE4**

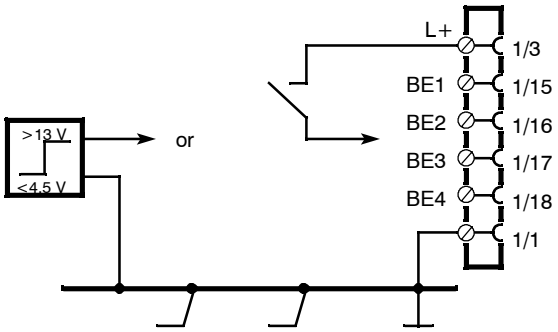


Figure 2-8 BE1 to BE4 wiring diagram

- **BA1 to BA8**

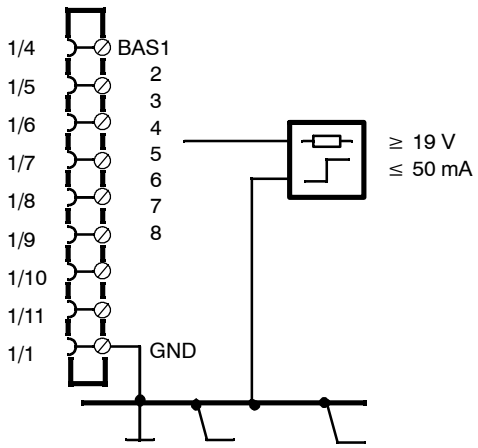
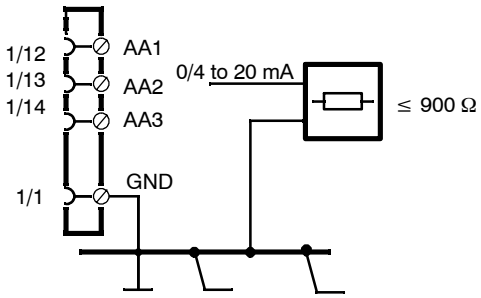


Figure 2-9 BA1 to BA8 wiring diagram

If S-controllers CSi* or CSE* are defined in the complex functions, the Δy outputs of the S-controllers are permanently assigned to the digital outputs BA*. See also BAx.1 Assignment via PUM1 ... 4.

Arithmetic block	+Δy/terminal	–Δy/terminal
h01.F	BA5 : 1/8	BA6 : 1/9
h02.F	BA7 : 1/10	BA8 : 1/11
h03.F	BA3 : 1/6	BA4 : 1/7
h04.F	BA1 : 1/4	BA2 : 1/5

- **AA1 to AA3**



Set AA 1 to AA 3 to 0 or 4 mA in hdEF

Figure 2-10 AA1 to AA3 wiring diagram

- **L+ (auxiliary voltage output)**

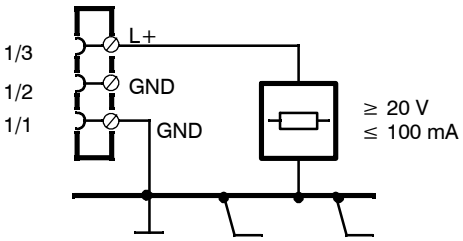


Figure 2-11 L+ connection

2.2.3 Wiring of the Option Modules

- **6DR2800-8A 3AE, U or I input**

  Slot 5: Set AE9 to AE11 in hdEF oP 5 to 3AE
  Set AE9 to AE11 in hdEF to 0 or 4 mA

  Slot 6: Set AE6 to AE8 in hdEF oP 6 to 3AE
  Set AE6 to AE8 in hdEF to 0 or 4 mA

  - Wiring

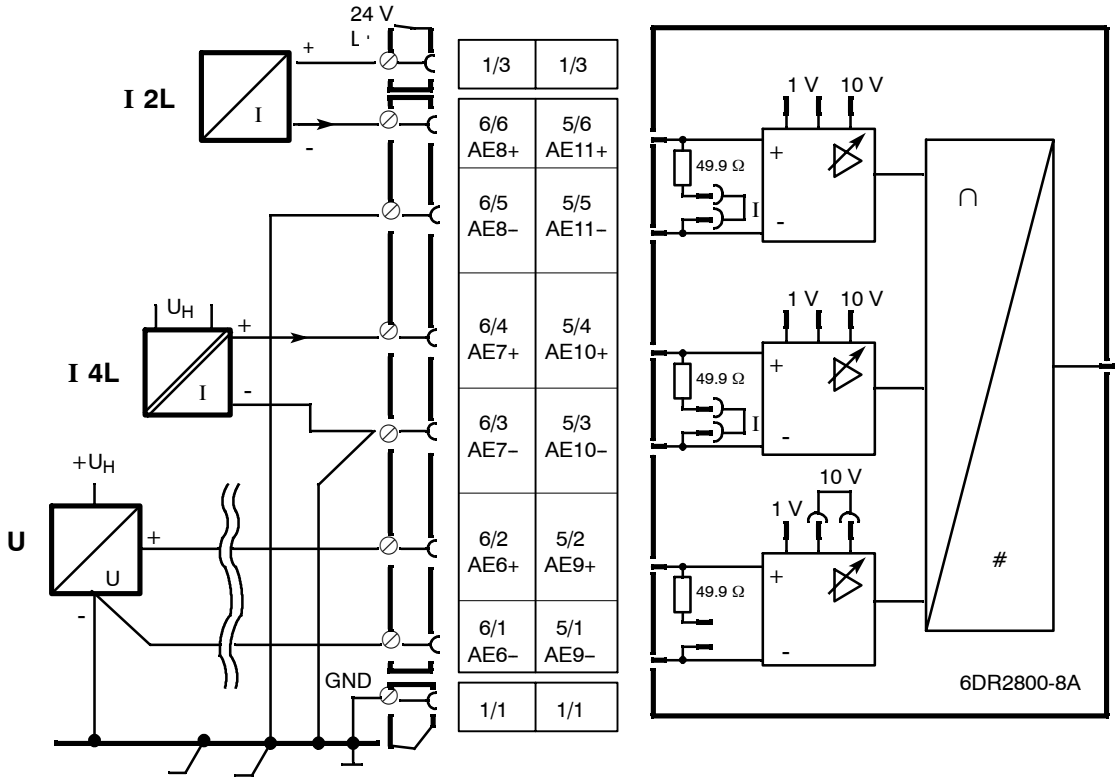


Figure 2-12 Wiring of 3AE module 6DR2800-8A

  - Jumper settings

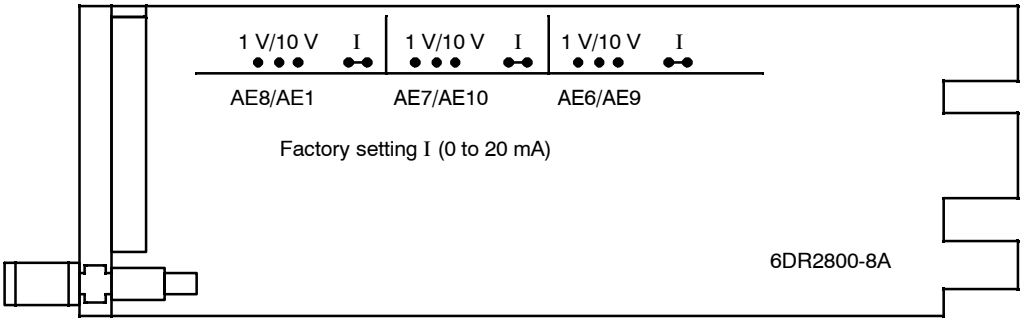
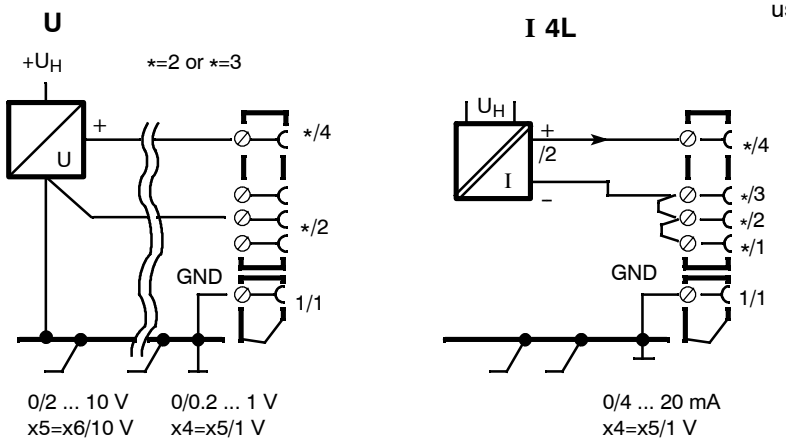


Figure 2-13 AE6 to AE8 or AE9 to AE11 jumper settings

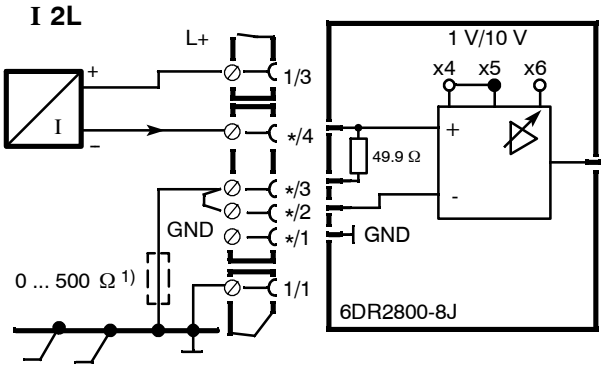
- **6DR2800-8J 1AE, U or Input**

AE4 in slot 2, set AE4 to 0 or 4 mA in hdEF
AE5 in slot 3, set AE5 to 0 or 4 mA in hdEF

Measuring ranges:
0 to 1 V/10 V/20 mA or
0.2 V/2 V/4 mA to
1 V/10 V/20 mA, plus 1 V/10 V
using jumpers on board



Factory setting 1 V, x4=x5 (and x7=x8)



1) potential load impedance from additional instruments

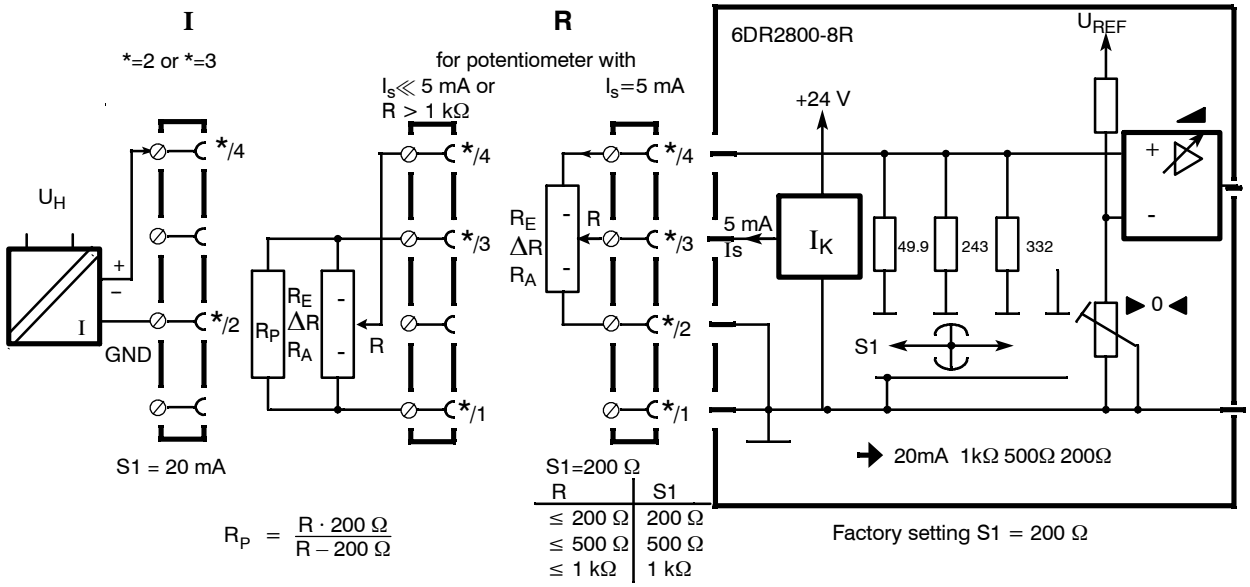
Alternative wiring, see chapter 2.2.4, page 123

Figure 2-14 Wiring of U/I module 6DR2800-8J

- **6DR2800-8R 1AE, resistance input**

  AE4 in slot 2; Set AE4 to 0 mA in hdEF
  AE5 in slot 3; Set AE5 to 0 mA in hdEF

- Wiring



$$R_P = \frac{R \cdot 200\ \Omega}{R - 200\ \Omega}$$

R	S1
≤ 200 Ω	200 Ω
≤ 500 Ω	500 Ω
≤ 1 kΩ	1 kΩ

Figure 2-15 Wiring of R module 6DR2800-8R

- Calibration

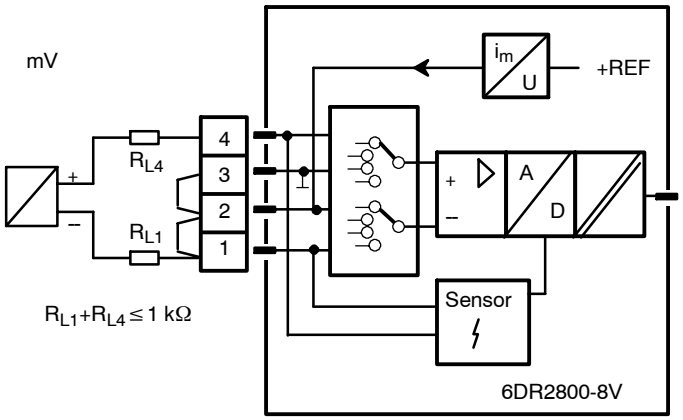
1. Set sliding switch S1 according to the measuring range
2. Set R_A using ▶ 0 ◀ display or analog output (configure accordingly) to start–of–scale value or 4 mA.
3. Set R_E using ◢ display or analog output to full–scale value or 20 mA.

- **6DR2800-8V universal module for analog input**

  The universal module can be plugged into slot 2 (analog input AE4) and slot 3 (analog input AE5). The measuring ranges are set using the menu CAE4/CAE5.

  - **Pin assignment for mV transmitter**

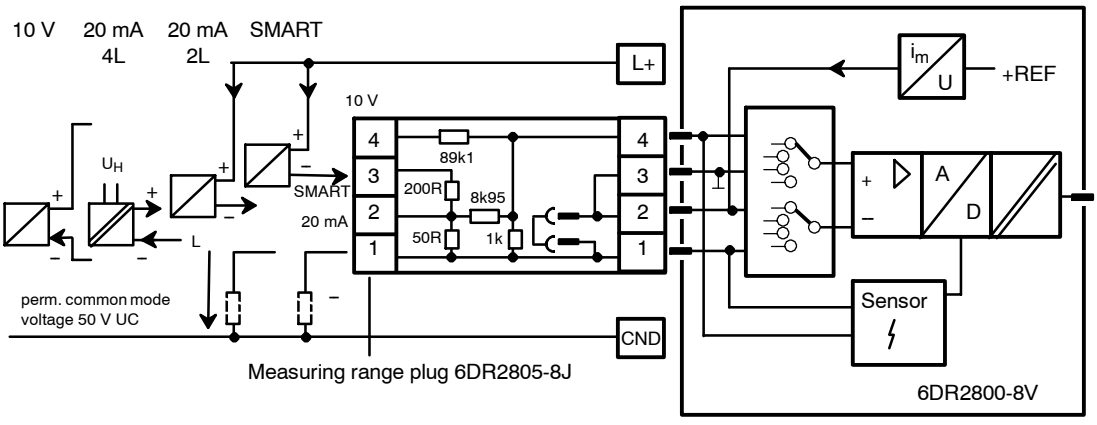
    Direct input Umax = ±175 mV



Block diagram of the mV module 6DR2800-8V

Figure 2-16 Wiring of UNI module

  - **Pin assignment measuring range plug 6DR2805-8J for U or I**



Block diagram of mV module 6DR2800-8V

Figure 2-17 Wiring of UNI module

- **Pin assignment for thermocouple TC**

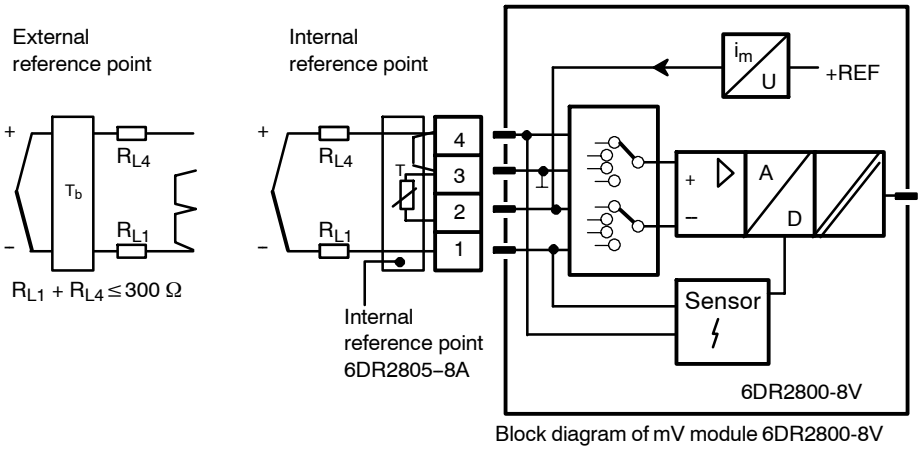


Figure 2-18 Wiring of thermocouple TC

- **Pin assignment for Pt100 sensor RTD**

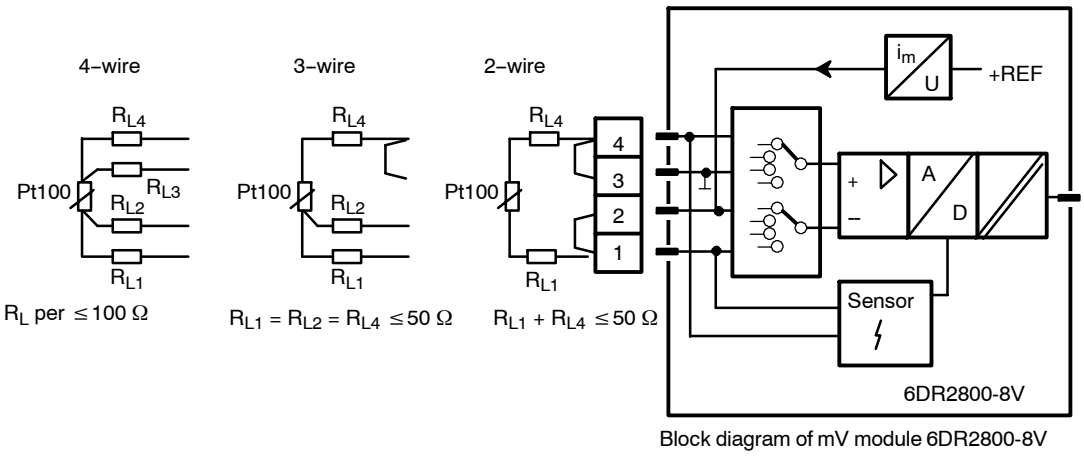
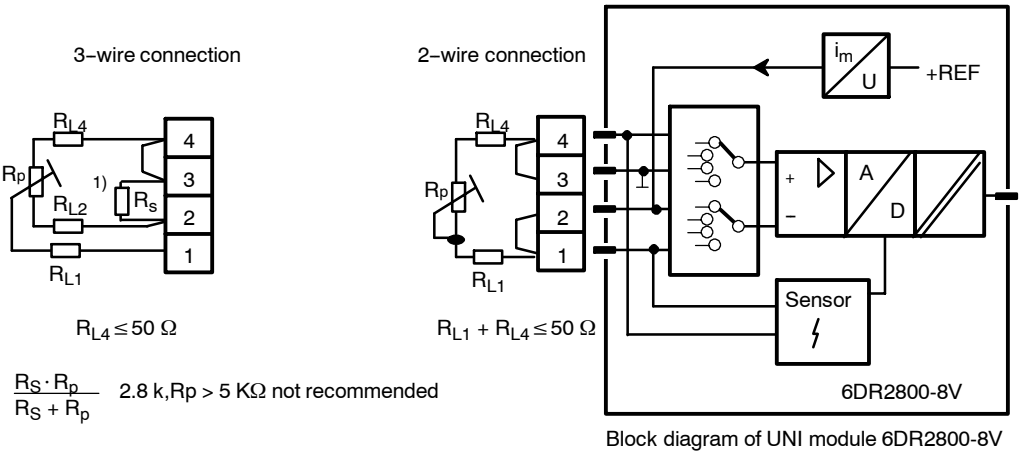


Figure 2-19 Wiring of PT100 sensor RTD

- **Pin assignment for resistance transmitter R**



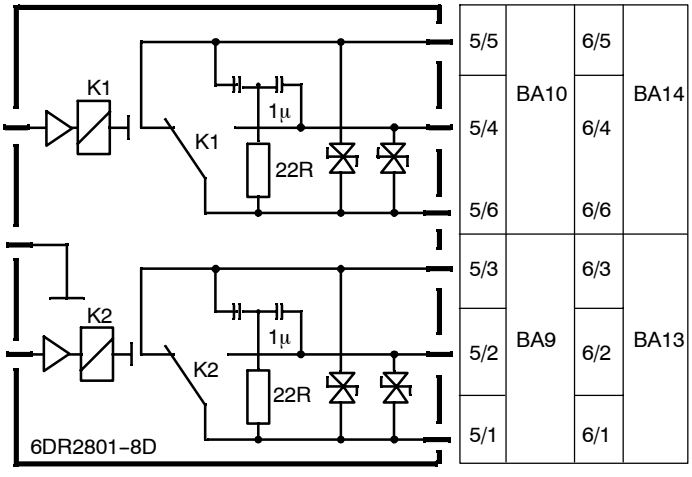
Block diagram of UNI module 6DR2800-8V

1) R_s jumper impedance only necessary if 2.8 kΩ < R ≤ 5 kΩ

Figure 2-20 Wiring of UNI module

- **6DR2801-8D 2BA relay 35 V**

BA9 and BA10 in slot 5, Set oP5 to 2 rEL in hdEF
BA13 and BA14 in slot 6, Set oP6 to 2 rEL in hdEF
Also see BAx assignment on page 114.



AC	≤	35	V	DC	≤	35	V
	≤	5	A		≤	5	A
	≤	150	VA		≤	80	W at 35 V
						100	W at 24 V

Figure 2-21 Wiring of 2BA (relay) module 6DR2801-8D

- **6DR2801-8E 4BA 24 V + 2BE**

BA9 to BA12 and BE5 to BE6 in slot 5, Set oP5 to 4bA in hdEF
BA13 to BA16 and BE10 to BE11 in slot 6, Set oP6 to 4bA in hdEF

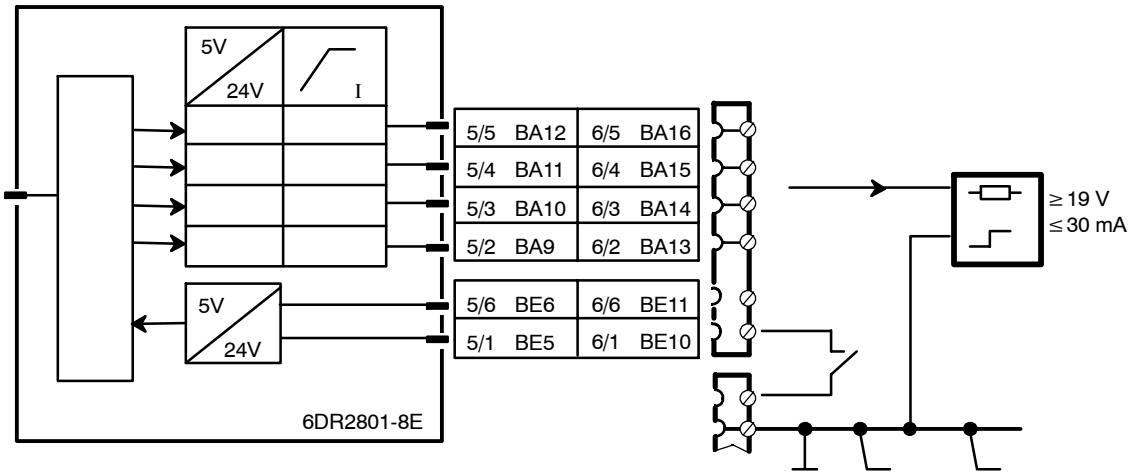


Figure 2-22 Wiring of 4BA (24 V) module 6DR2801-8E

- **6DR2801-8C 5BE**

BE5 to BE9 in slot 5, Set oP5 to 5bE in hdEF
BE10 to BE14 in slot 6, Set oP6 to 5bE in hdEF

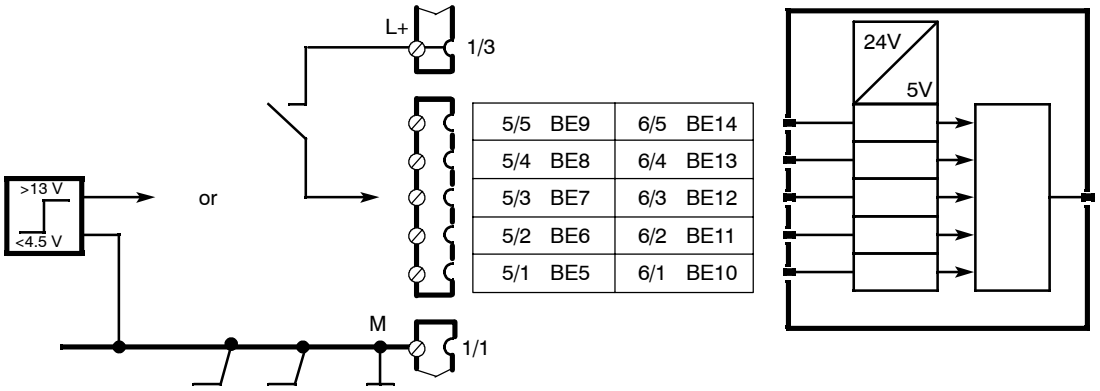
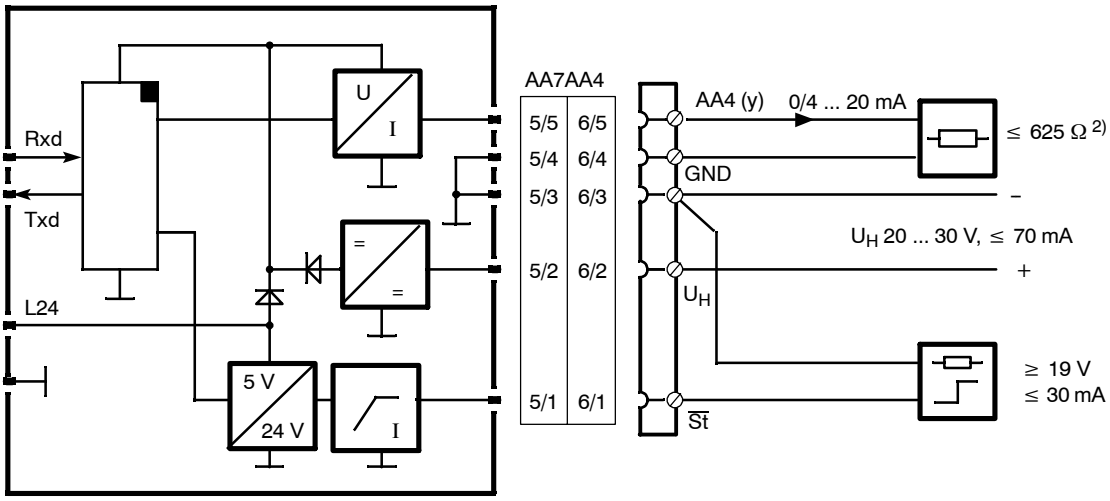


Figure 2-23 Wiring of 5BE module 6DR2801-8C

- **6DR2802-8A (1AA, y_{hold})**

AA7 in slot 5 Set oP5 to 1AA in hdEF
AA4 in slot 6 Set oP6 to 1AA in hdEF



1) UH need only be connected if the output current is to be maintained even in the event of a power failure in the controller or when removing the module for service work.
2) Up to 900 Ω possible depending on the supply (see chapter 1.6.3, page 99).

Figure 2-24 Wiring of y_{hold} module 6DR2802-8A

- **6DR2802-8B 3AA + 3BE**

AA7 to AA9 and BE5 to BE7 in slot 5
AA4 to AA6 and BE10 to BE12 in slot 6

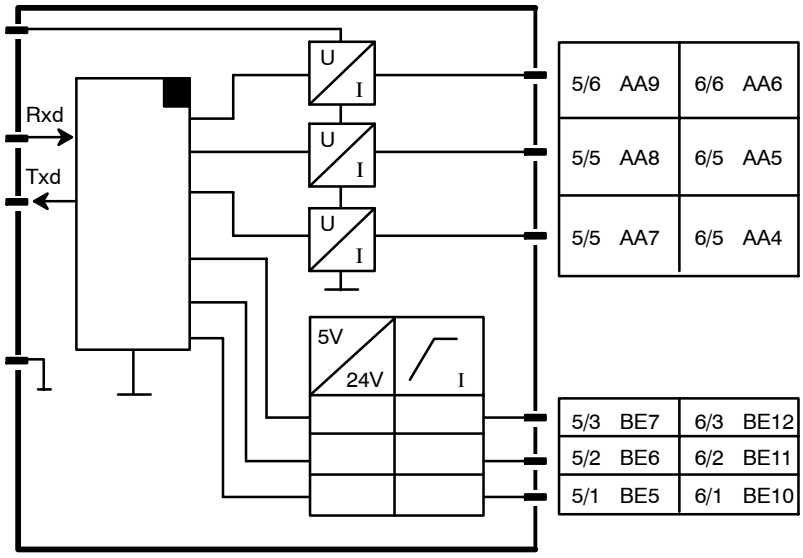


Figure 2-25 Wiring 3AA/3BE module 6DR2802-8B

- **6DR2804-8A (interface relay 230 V, 4 relays)**
  6DR2804-8B (interface relay 230 V, 2 relays)

E.g. wiring for ±Δy outputs in the S-controller with interface relay 230 V, 2 relays (6DR2804-8B)

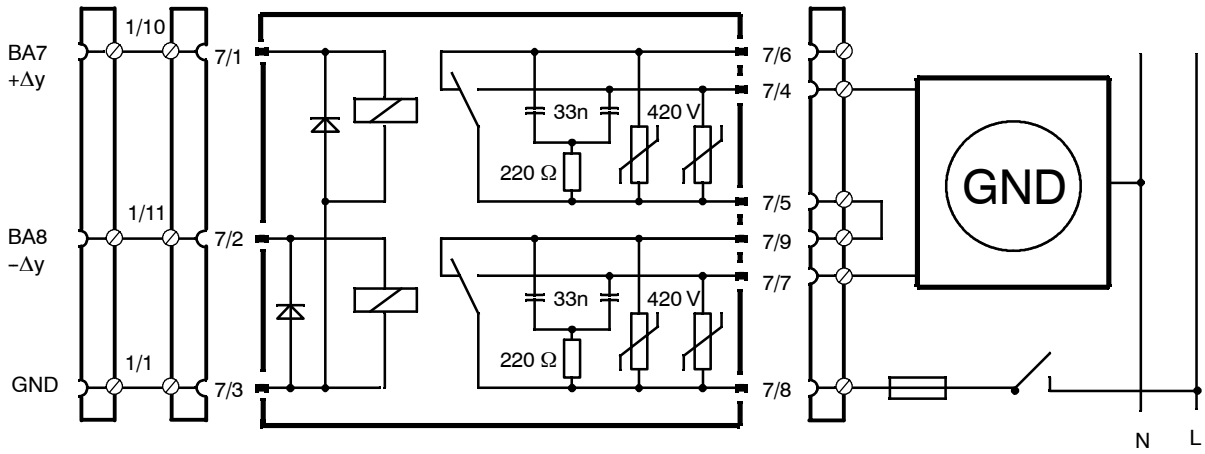


Figure 2-26 Wiring of interface relay 230 V 6DR2804-8B

The interface relay 230 V, 4 relays (6DR2804-8A) contains 4 relays. Terminals 8/1 to 8/9 must then be connected accordingly in addition to the terminals 7/1 to 7/8.

Attention: Observe the max. switching voltage! (resonance sharpness in phase shift motors, see chapter 1.4.2, page 12)

AC	250	V	DC	250	V
	8	A		8	A
	1250	VA		30	W at 250 V
				100	W at 24 V

2.2.4 Alternative Wiring for I- and U Input

- **0/4 to 20 mA signals**

  The 49.9 Ω input impedance is connected across the input signals AE+ and AE− (AE1 to AE3 in the standard controller and in module 6DR2800-8A by means of jumper settings and by external wiring on the option module for AE4 and AE5).
  If the signal is still required during service work in which the terminal is disconnected, the 49.9 Ω ±0.1 % input impedance must be connected to the terminal between AE+ and AE−. The internal 49.9 Ω resistance must then be disconnected by appropriate jumper settings or by rewiring.

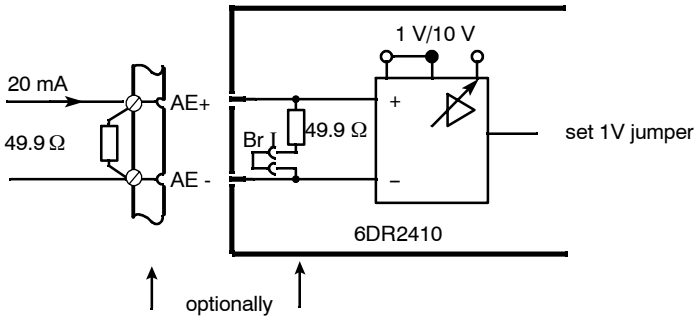


Figure 2-27 Signal input AE1 to AE3 of the standard controller, internal or external 49.9 Ω resistance or signal input AE6 to AE8 via module 3AE, 6DR2800-8A

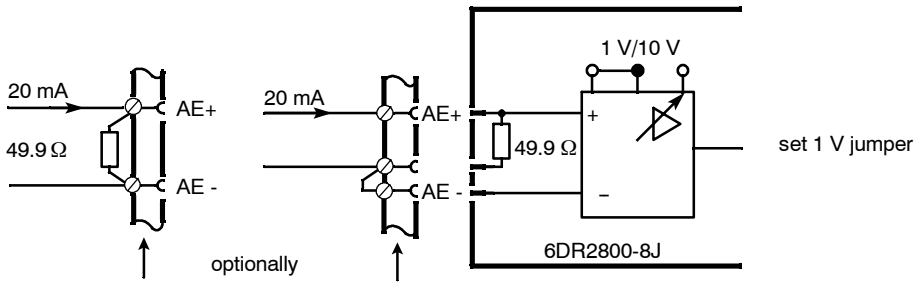


Figure 2-28 Signal input AE4, AE5 via option module 6DR2800-8J, internal or external 49.9 Ω resistance

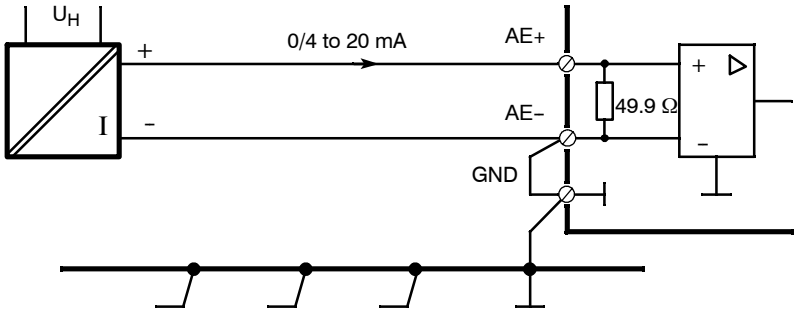


Figure 2-29 Connection of a 4-wire transmitter 0/4 to 20 mA with potential isolation

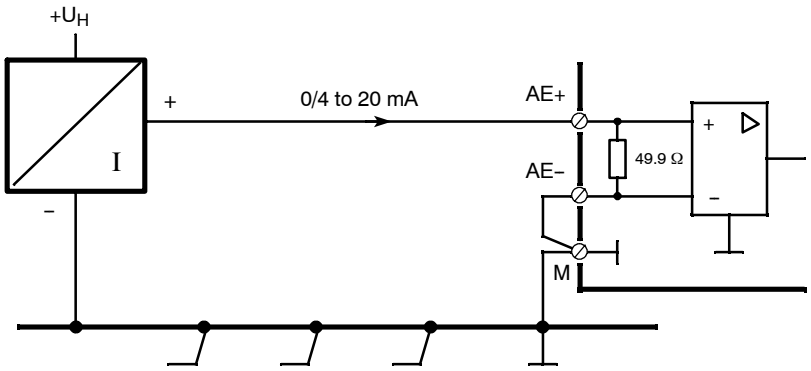


Figure 2-30 Connection of a 3-wire transmitter 0/4 to 20 mA with negative polarity to ground

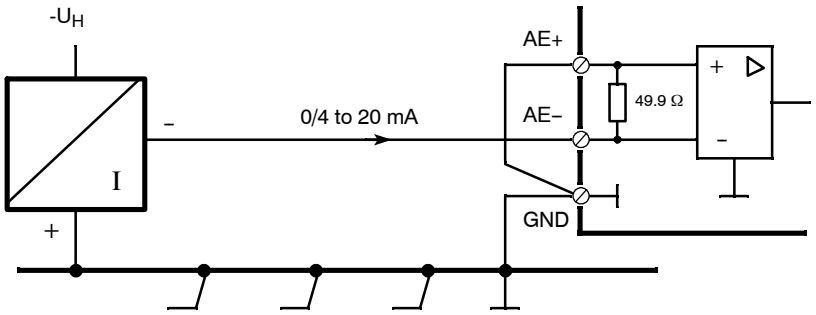


Figure 2-31 Connection of a 3-wire transmitter 0/4 to 20 mA with positive polarity to ground

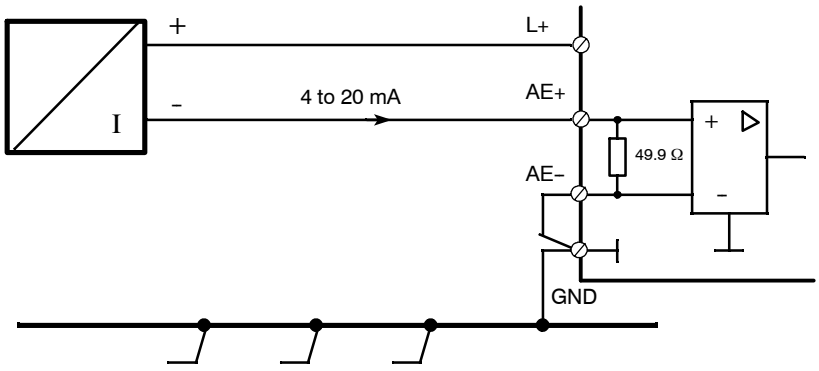


Figure 2-32 Connection of a 2–wire transmitter 4 to 20 mA supplied from controller's L+

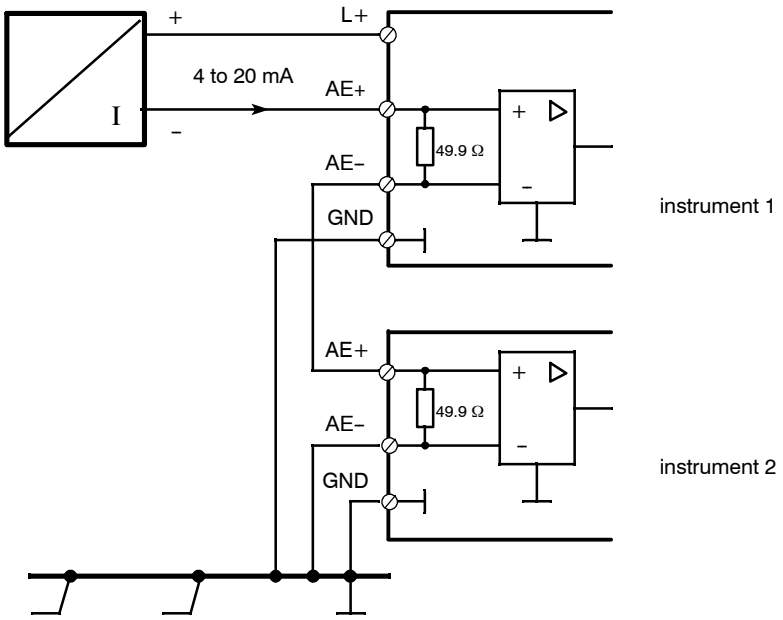


Figure 2-33 Connection of a 2-wire transmitter 4 to 20 mA to two instruments in series and supplied by L+ from one of the instruments

Every input amplifier is supplied by a differential voltage of 0.2 to 1 V. Instrument 1 also has a 0.2 to 1 V common–mode voltage that is suppressed in this case. Several instruments with a total common–mode voltage of up to 10 V can be connected in series. As the last instrument's input is connected to ground, its input impedance is referred to ground.

As there will be an increased impedance (maximum permissible common–mode voltage +10 V), the permissible impedance voltage of the transmitter or the on–load voltage may not be exceeded!

- **Voltages 0/0.2 to 1 V or 0/2 to 10 V**

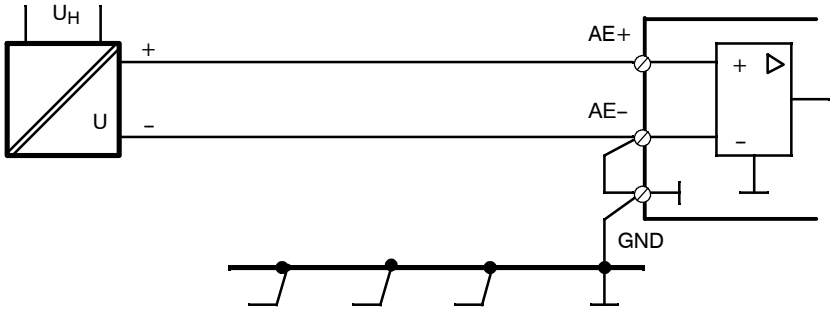


Figure 2-34 Wiring of a floating voltage supply

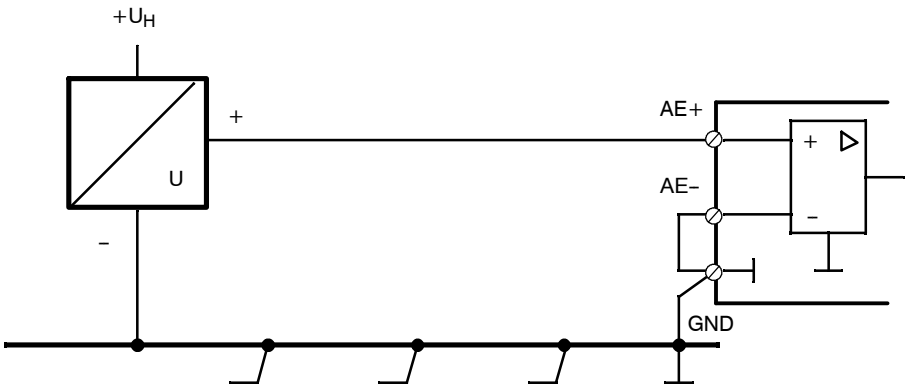


Figure 2-35 Single–pin wiring of a non–floating voltage supply with negative polarity to ground

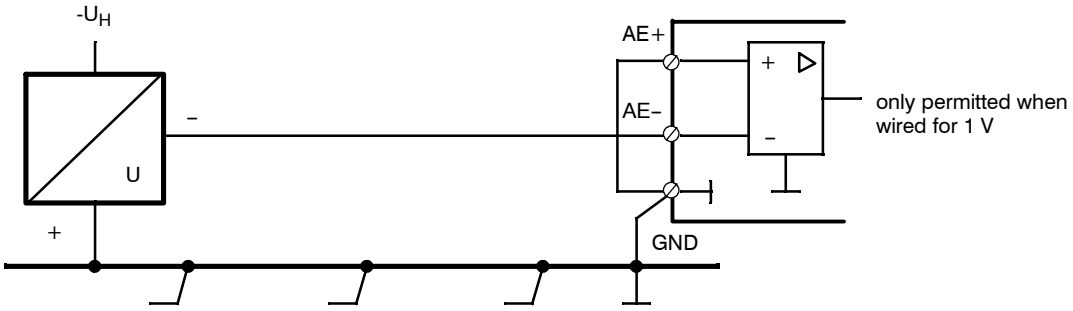


Figure 2-36 Single–pin wiring of a non–floating voltage supply with positive polarity to ground

Figure 2-35 and Figure 2-36:
The voltage dip on the ground rail between the voltage source and the input amplifier appears as a measuring error. Only use when ground cables are short or choose a circuit configuration as shown in figure 2-37!

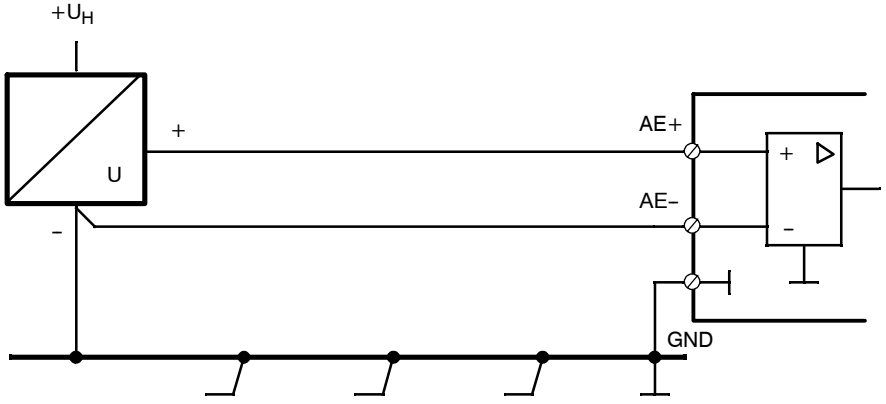


Figure 2-37 Double–pin wiring of a voltage source with positive polarity to ground

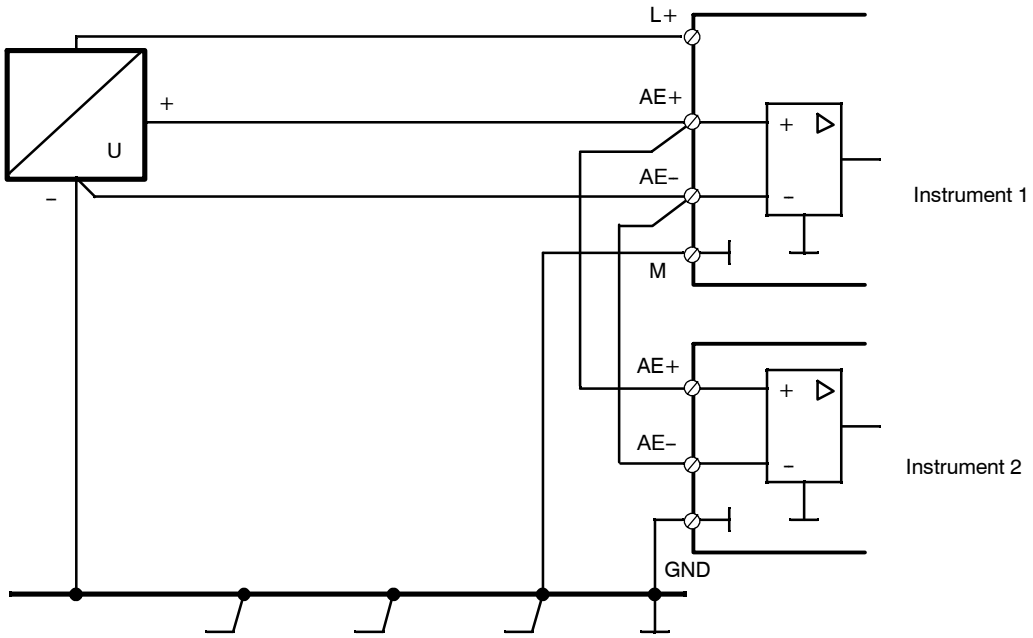


Figure 2-38 Parallel wiring of a non–floating voltage supply to two instruments. The voltage source is supplied by L+ of one of the instruments and negative polarity is referred to ground.

Figure 2-37 and Figure 2-38:
The voltage dip on the ground rail between the voltage source and the input amplifier appears as a common mode voltage and is suppressed.

2.2.5 Wiring of the Interface

- **Wiring of the interface module 6DR2803-8C**

  - **RS 232 point–to–point (END/END)**
    Can be inserted in slot 4

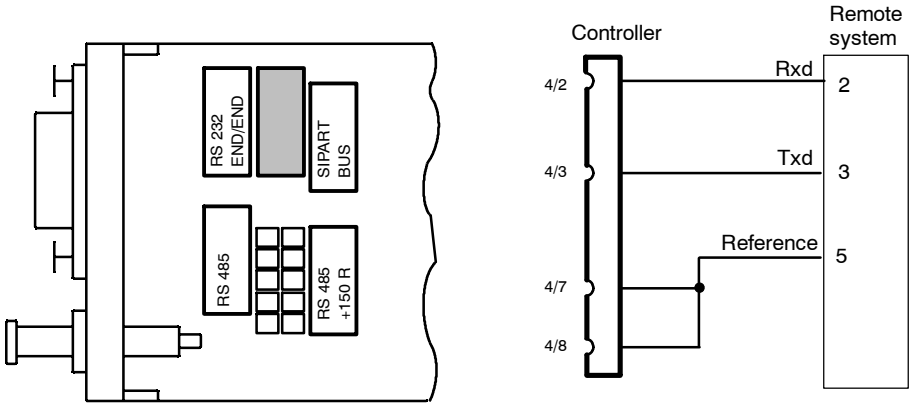


Figure 2-39 Setting on the SES module 6DR2803-8C with RS 232 point–to–point and wiring

- **RS 485 bus**
  Can be inserted in slot 4

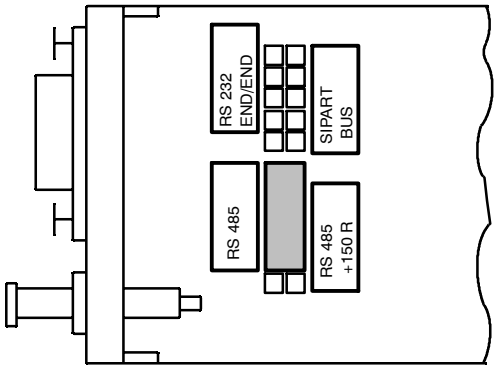


Figure 2-40 Jumper settings SES module 6DR2803-8C at RS 485 bus

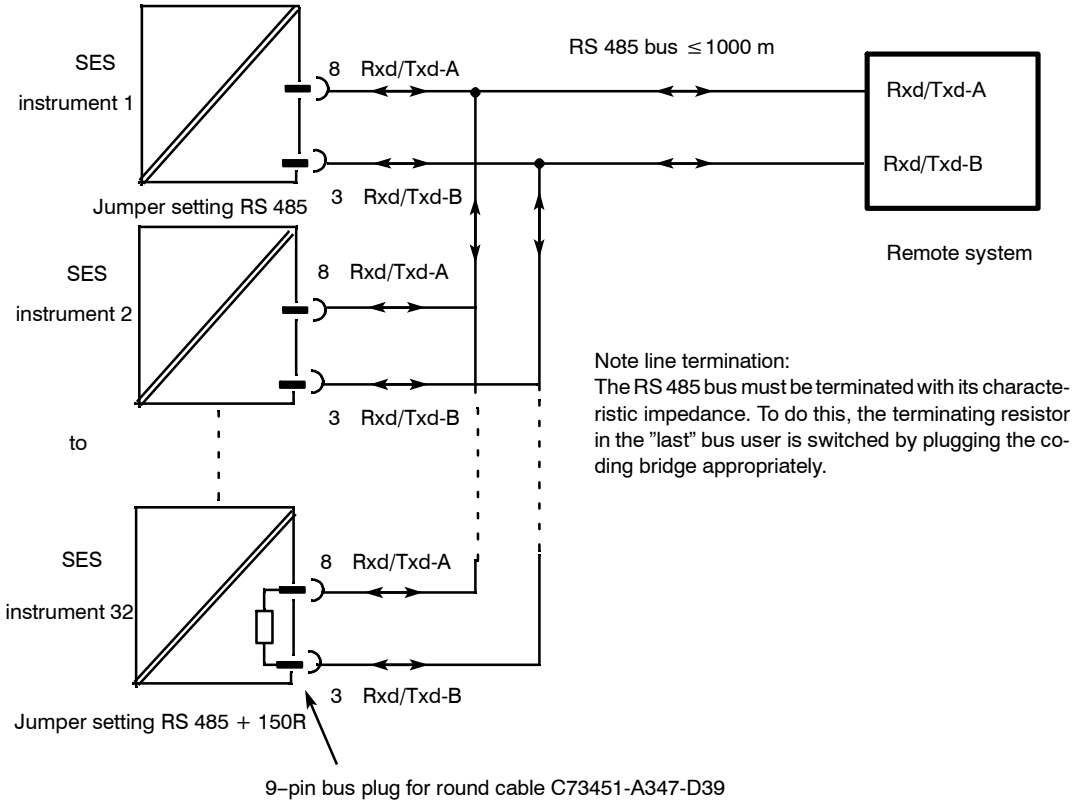
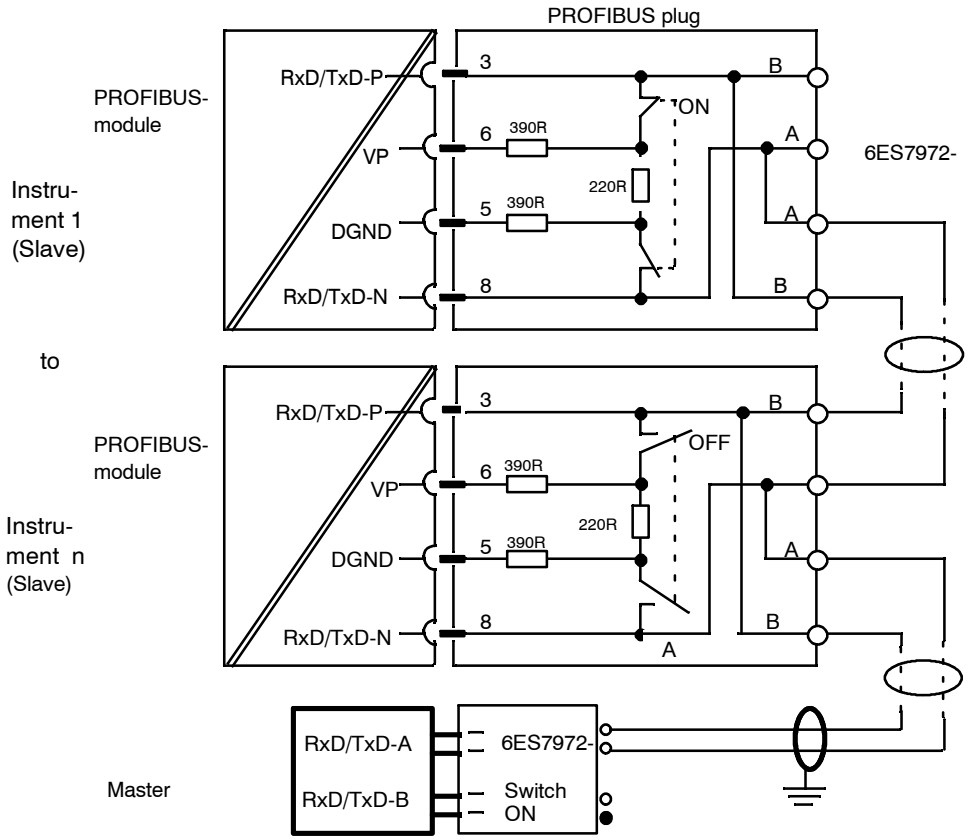


Figure 2-41 Wiring of RS 485 bus

- **Wiring the interface PROFIBUS-DP, 6DR2803-8P**

Wiring

Can be inserted in slot 4



max. number of controllers, without Repeater: 32
max. number of bus users (Slave + Master): 126

Figure 2-42 Principle diagram SIPART DR24 via PROFIBUS-DP and bus plug to master

Note line termination:

The RS 485 bus must be terminated with a characteristic impedance. To do this, the switch in the bus connector must be switched ”ON” in the ”first” and ”last” bus users. The switch may not be ”ON” in any of the other bus users. A detailed description and notes on cable laying and bus cable laying can be found in the Manual Decentral Peripheral System ET200.
Order number 6ES5 998-3ES12.

3 Operation

The SIPART DR24 is operated exclusively and fully with the operating keys on the front module. The function of the operating panel can be switched between three main modes:

- Process operation mode
- Selection mode
- Configuring mode

Some of the keys and displays on the front module are assigned different control and display functions when the operating mode is changed. See the description of the respective main mode for details.

Figure 3-1 Connectable control and display elements in the process operation mode and fixed assignment in parameterization/configuring (see page 3)

3.1 Process Operation Mode

The function of the keys, LEDs and displays is defined by the respective user program in the process operation mode.

The enclosed label must be labelled with the appropriate function of the keys, LEDs and displays and inserted underneath the foil on the front (see also chapter 5, page 169).

The measuring point label is changeable. To change it, open the plexiglass cover with a pointed tool in the center and take out the label. The screw becomes visible with which the front module is fixed to the controller (see chapter 5, page 169).

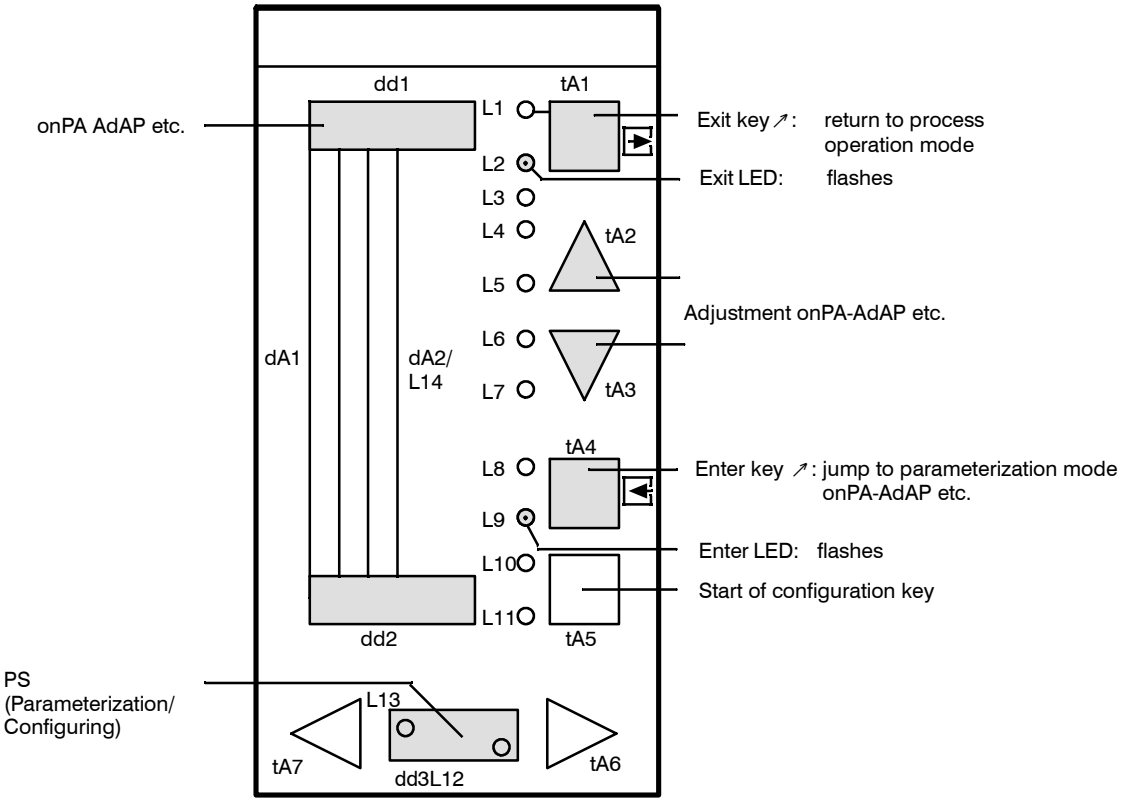
3.2 Selection Mode

You enter the selection mode for the various configuration menus by pressing the Shift key (6) for longer (approx. 5 s) until the “PS” mark is flashing in the dd3 display.

Condition: Digital signal ”Block-Operate” bLb = 0 and
”Block-Parameterize, Structure” bLPS = 0

The controller operates in online mode in the selection mode, i.e. its last operating mode is retained, the current process variables can be traced on the analog displays (1), (2).

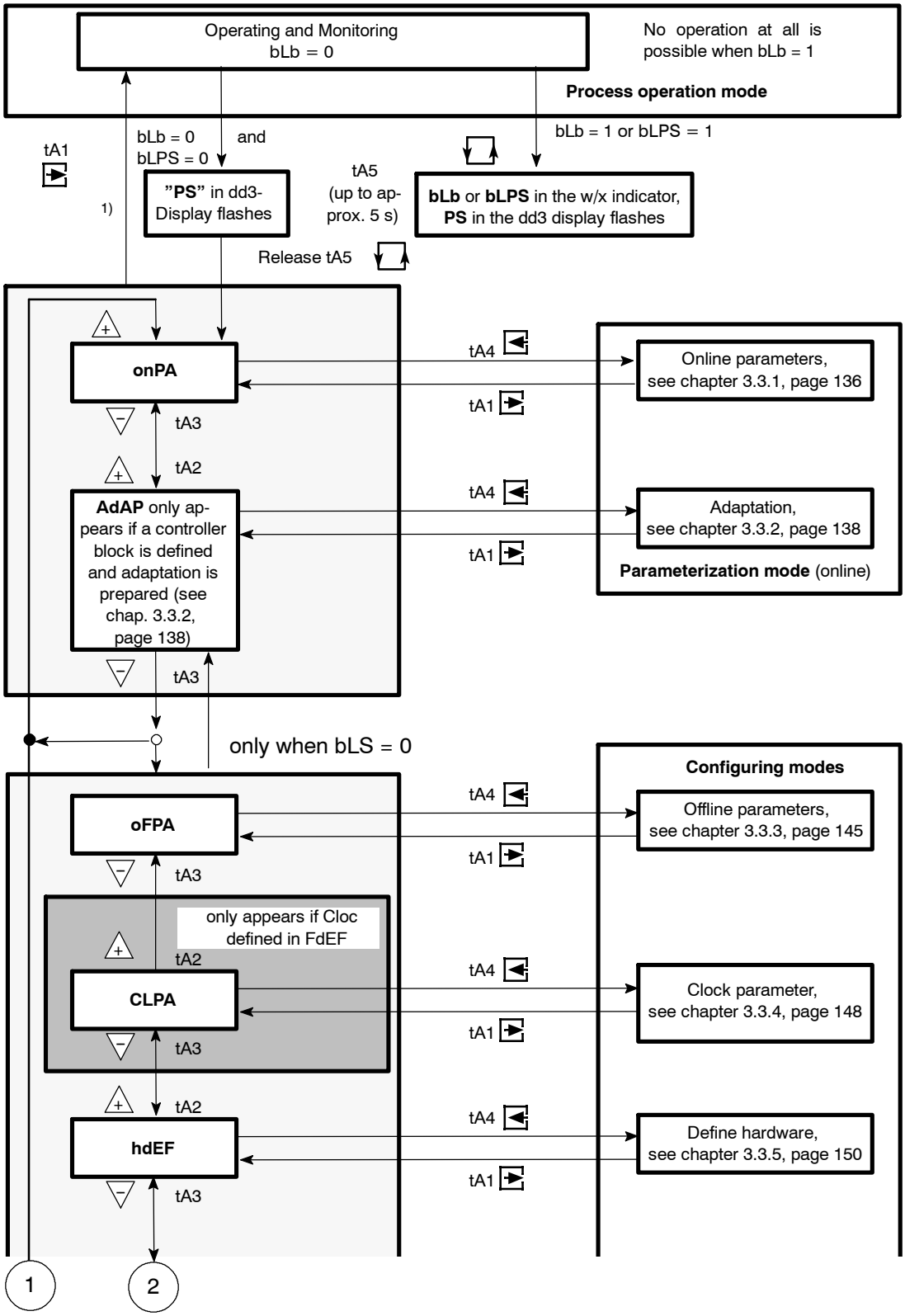
The configuration menus can be selected with tA2, tA3. The controller automatically returns to the process operation mode if neither of these menus is called with the Enter key (11) (≙ Enter configuration level) within about 20 s.



1) AdAP appears if a controller is defined in FdEF in block h*.F, block h*.F is positioned in FPoS, the control input AV = High.

All unlabelled control and display elements have the function corresponding to the user program.

Figure 3-2 Control and display elements in the selection mode


Operating and Monitoring
bLb = 0
No operation at all is possible when bLb = 1
Process operation mode
bLb = 0 and bLPS = 0
bLb = 1 or bLPS = 1
tA1
1)
"PS" in dd3-Display flashes
tA5 (up to approx. 5 s)
bLb or bLPS in the w/x indicator, PS in the dd3 display flashes
Release tA5
onPA
tA4
tA1
tA3
tA2
AdAP only appears if a controller block is defined and adaptation is prepared (see chap. 3.3.2, page 138)
Online parameters, see chapter 3.3.1, page 136
Adaptation, see chapter 3.3.2, page 138
Parameterization mode (online)
only when bLS = 0
Configuring modes
oFPA
Offline parameters, see chapter 3.3.3, page 145
only appears if Cloc defined in FdEF
CLPA
Clock parameter, see chapter 3.3.4, page 148
hdEF
Define hardware, see chapter 3.3.5, page 150
1
2

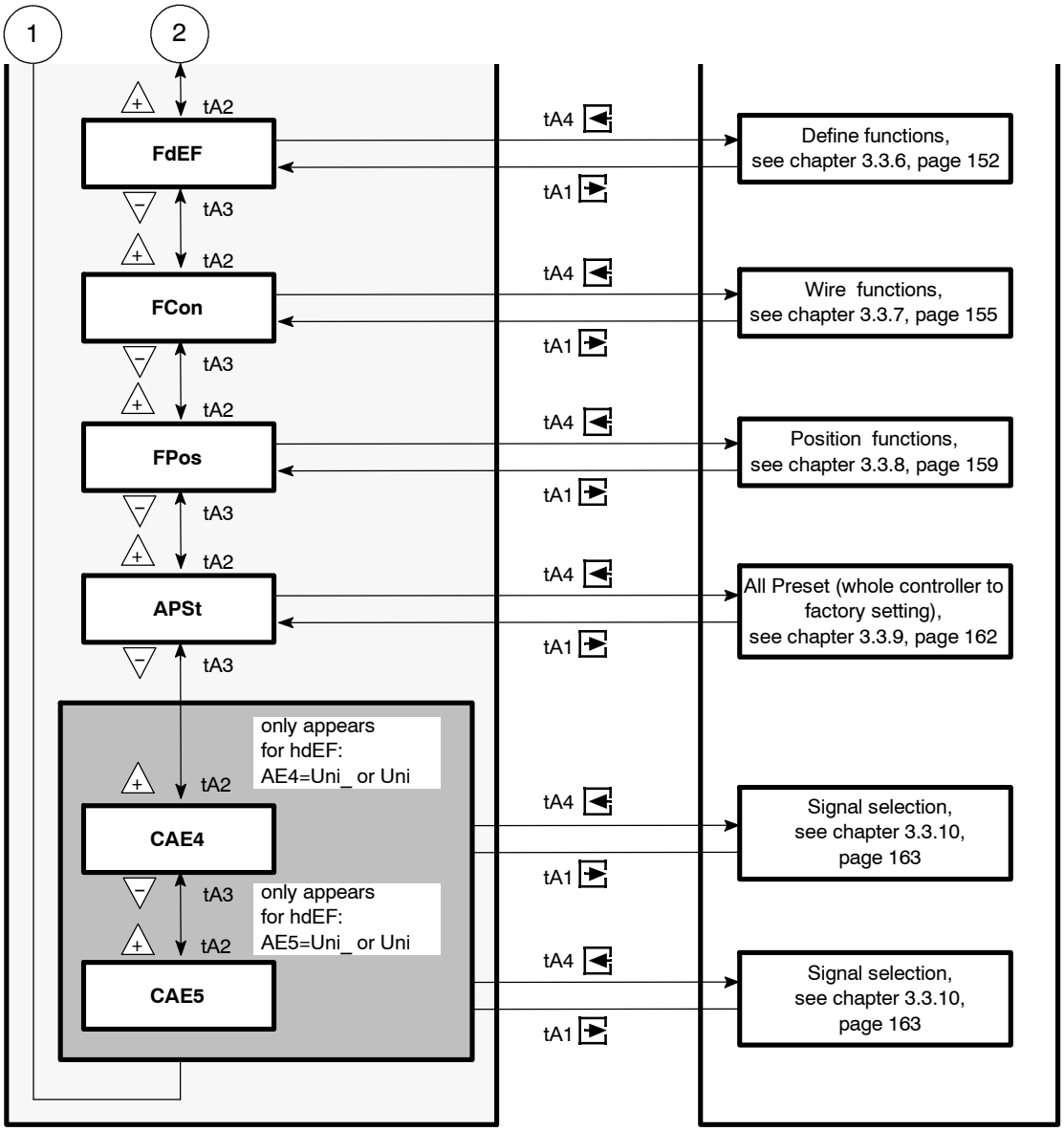


Figure 3-3 Selection mode

3.3 Configuring Mode (Parameterization and Configuring Mode)

The instrument settings are made in the configuring mode.

Settings in the ”Parameterization mode” onPA and AdAP can be made in online.

The settings in the ”Configuring mode” (oFPA, ... to CAE5) are made offline. The dA2 shows a striped pattern to identify the offline mode. The analog and digital outputs behave as described in chapter 1.5.3, page 29. The behavior of the analog and digital outputs can be varied with the data source nStr (no configuring) which is low during the individual structuring modes including the parameterization preselection mode.

The analog display dA1 and the LEDs L1, L3 to L8, L10 to L13 are dark and key tA5 has no function.

The key tA1 becomes the Exit key, the corresponding LED L2 indicates standby to exit. Whenever L2 flashes, pressing the Exit key causes a jump from the selected level to the next level up in the hierarchy.

Key tA4 becomes the Enter key, the corresponding LED L9 indicates standby to enter. Whenever L9 flashes, pressing the Enter key causes a jump to the next level down in the hierarchy (pre–selection level –> configuring level, e.g. onPA)

The keys tA2 and tA3 serve to adjust the variables (mode name, answer or parameter value) shown in the digital display dd1. The keys tA6/7 serve to adjust the variables (roLL–SEt, question, function name and parameter name) shown in the digital displays dd2 and dd3.

The question and answer cycles, the parameter names and the parameter values with a large number range can be adjusted with a fast action in the structuring modes oFPA, CLPA, hdEF, FdEF, FCon, FPoS. To do this, first the adjustment direction is selected with tA2 or tA3 or tA6 or tA7 and then the fast action switched on by pressing the other direction key. The operating mode roLL or SEt is selected with tA6/7 in the configuring preselection level. Adjustment of the parameter value or the answer cycle is only possible in the individual configuring modes in the SEt operating mode. The adjusting keys tA2/3 are blocked in the roLL operating mode. This enables offline parameters, function definitions or wirings to be viewed for example without having to fear accidental adjustment of the entered data.

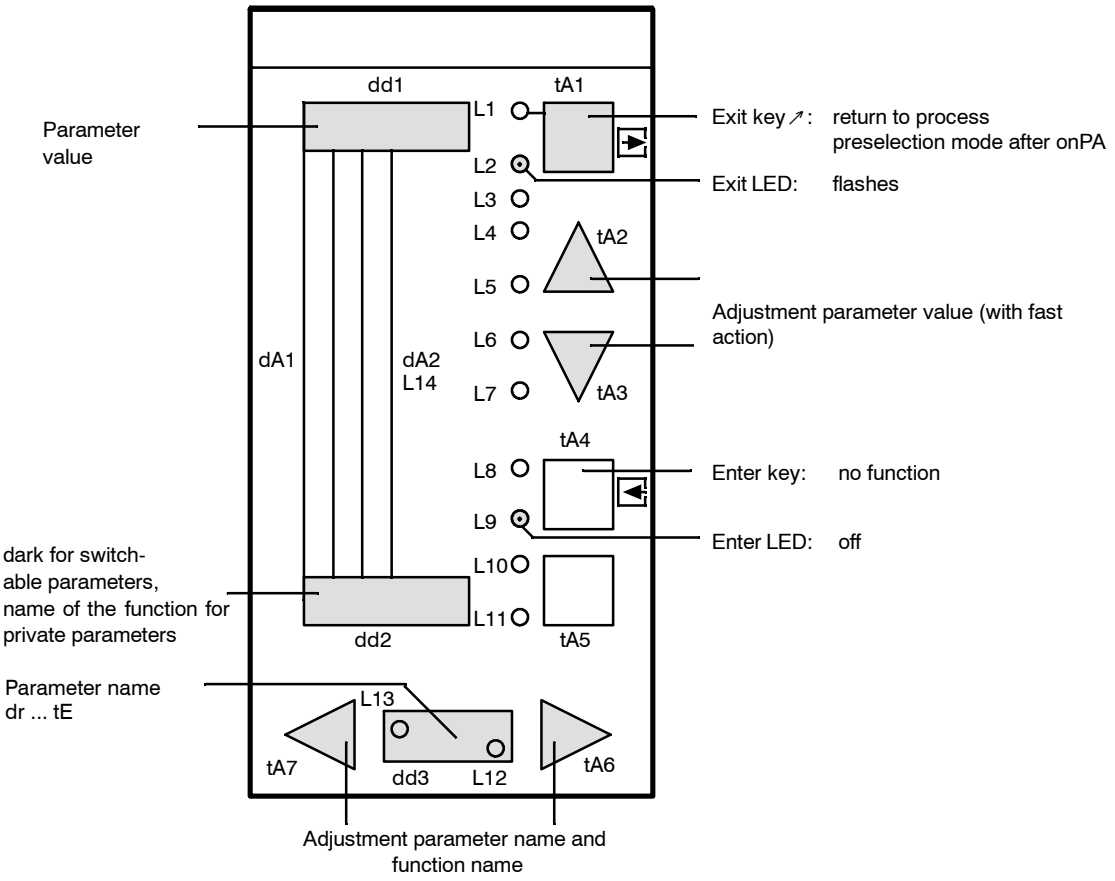
After exiting the paramterization mode, the data are saved in the non–volatile user program memory and the SIPART DR24 switches to online mode. If changes have been made in the configuring modes hdEF, FdEF, FCon, FPoS, the counting, timing and memory functions react like for a Power–on reset with batt = no. The outputs are set to the values/states specified for the individual functions.

It is possible to block the parameterization or configuring modes through the data sinks bLb (Block operation), bLPS (Block parameterization/configuring) and bLS (Blocking configuring) (see chapter 3.2, page 131 and figure 3-3, page 134).

3.3.1 Parameterization Mode onPA (Online Parameters)

In the parameterization mode onPA the parameters are arranged whose effect on the process when they are changed can be observed. The other parameters are arranged in the configuring modes oFPA and CLPA (see chapter 3.3.3, page 145 and 3.3.4, page 148).

The online parameters are listed in table 1. The parameters against a white background (repetition rate dr for the digital displays and the switchable decadic (Pd) and linear parameters (PL) are always accessible. The parameters against a gray background are the private parameters of the complex functions and only appear when the functions are defined in FdEF.



All unnamed control and display elements have the wired function

Figure 3-4 Control and display elements in the parameterization mode onPA

dd2	dd3	dd1 Setting range	Factory setting	Resolu-tion	Dimen-sion	Parameter meaning	
dd1.1						Digital display 1 input 1	
dd1.2						Digital display 1 input 2	
dd1.3						Digital display 1 input 3	
dd1.4						Digital display 1 input 4	
dd2.1						Digital display 2 input 1	
dd2.2	dr	1 to 100	1	1	Cycles / Display	Digital display 2 input 2	Repetition
dd2.3						Digital display 2 input 3	rate
dd2.4						Digital display 2 input 4	
dd3.1						Digital display 3 input 1	
dd3.2						Digital display 3 input 2	
dd3.3						Digital display 3 input 3	
dd3.4						Digital display 3 input 4	
Pd10	–					switchable decadic parameters	1
↓		0.100 to 9984	10.00	128 values / Octave	1, s. 100 %		↓
Pd40	–						40
PL01	–					switchable linear parameters	1
↓		–1.999 to 19.999	0.000	0.001	1, s. 100 %		
PL40	–						40
tAC1	PEr	2 to 10000	2	1	Cycles	Clock signal 1	period duration
↓							
tAC2	tAS	1 to 10000	1	1		Clock signal 2	turn–on time
AFi1						Adaptive filter 1	
↓	tF	oFF, 1.000 to 9984	1.000	128 values / Octave	s		time constant
AFi2						Adaptive filter 2	
Ain1	tin	1.000 to 9984	10.00	128 values / Octave	s	Analog integrator 1	integrating time
↓	tr	oFF, 1.000 to 9984	oFF		s		follow–up time (ramp)
	Lia 2)	–199.9 to 199.9	–5.0		%		output limit start
Ain4	LiE 2)	–199.9 to 199.9	105.0	0.1	%	4	output limit end
bin1	tin	ProG, 1 to 9984	ProG	128 values / Octave	s	Digital integrator 1	integrating time
↓	tr	oFF, 1.000 to 9984	oFF		s		follow–up time (ramp)
	Lia 2)	–199.9 to 199.9	–5.0		%		output limit start
bin6	LiE 2)	–199.9 to 199.9	105.0	0.1	%	6	output limit end
Ccn1	cP	0.100 to 100.0	0.100	0.001	1	Controller K 1	proportional action factor
or 1)	tn	0.100 to 9984	9984		s	or	integral action time
CSE1	tv	oFF, 1.000 to 2992	oFF	128 values / Octave	s	Controller S external 1	derivative action time
or 1)	vv	0.100 to 10.00	5.0		1	or	derivative gain
CSi1	AH	0.0 to 10.0	0.0	0.1	%	Controller S internal 1	response threshold
↓	Yo	AUto, 0.0 to 100.0	AUto	0.1	%		working point P–con troller
Ccn4	YA 2)	–10.0 to 110.0	–5.0	0.1	%	Controller K 4	actuating value limit start
or 1)	YE 2)	–10.0 to 110.0	105.0	0.1	%	or	actuating value limit end
CSE4	tY	10 to 1000	60		s	Controller S external 4	actuating time
or 1)	tA	20 to 600	180	128 values / Octave	ms	or	min. actuating pulse pause
CSi4	tE	20 to 600	180	20	ms	Controller S internal 4	min. actuating pulse length

dd2	dd3	dd1 Setting range	Factory setting	Resolution	Dimension	Parameter meaning
dti1 ↓ dt12	td	oFF, 1.000 to 9984	1	128 values Octave	s	Dead time element 1 dead time Dead time element 2
PUM1 ↓ PUM4	tAE tM	20 to 9980 0.100 to 1000	20 0.100	20 128 values/octave	ms s	Pulse width modulator 1 reduces turn–on time 4 period duration
Spr1 ↓ Spr8	SPA SPE	0.0 to 100.0 0.0 to 100.0	0.0 100.0	0.1 0.1	% %	Split range 1 foot point 8 corner point

1) YE > YA, LiE > LiA

omitted if not defined in FdEF

Fast action jumps

Table 3-1 Online parameters in parameterization mode onPA

3.3.2 Parameterization Mode AdAP (Adaptation)

This mode appears in the parameter preselection mode **only** when the control input AV is High and the block is positioned in FPoS in **one** of the defined controllers (blocks h*.F). The Enter function into the parameterization mode AdAP can only be used if the controller selected for adaptation is in manual mode.

In the parameterization mode AdAP, the SIPART DR24 acts online on the process (but the corresponding controller is in manual mode).
The necessary process displays can be provided during adaptation by appropriate connection with the controller output AL (adaptation in progress) in connection with the indicators and switching functions.

The parameterization mode AdAP has 4 different statuses (described in detail below):

- pre adaptation
- during adaptation
- aborted adaptation
- post adaptation

The digital displays dd1 to dd3 and the keys get different functions in the individual statuses which can be included in the controller operating concept without any hitches.

The digital displays and the keys are used before and after adaptation for the parameter display and - setting as is the case in the parameterization and configuring modes onPA or oFPA (see figure 3-6, page 142).

The complete connected process image as described in chapter 3.1 is displayed during adaptation (see figure 3-7, page 142).

The error message flashes on dd1 and dd2 when adaptation is aborted. The error messages are acknowledged with the Enter key (see figure 3-7, page 142).

- **Pre adaptation**

The data source AdAP is low and may display readiness for adaptation when connected, for example with L13. First the parameters for the presettings (tU, dPv, dY) are displayed. They must be set according to the desired jump signal. Then the old parameters xx.o with the ID Pi or Pid with their value and the new parameters xx.n with the ID Strt AdAP appear on the displays. The old and the new parameters are not adjustable.

The adaptation can only be started with the Enter key (tA4) when the new parameters **.n with the display Strt AdAP are selected (manual operation is a prerequisite).

- **During adaptation**

The data source AdAP switches alternately between high and low and may display the current adaptation when connected for example with L3. The process can be monitored on the completely connected process display.

- **Aborted adaptation**

The data source AdAP is low and may display readiness for adaptation after error acknowledgement when connected for example with L3. The current adaptation can be aborted manually or automatically by the error monitor.

Manual abortion can be activated in the event of danger by pressing the Exit key (tA1). It then returns to the selection mode after AdAP. From there you can return to the process operation mode by pressing the Exit key (tA1) again. The controller is in manual mode and the manual manipulated variable can be adjusted if wired appropriately.

Automatic abortion is effected by the error monitors (see table 3–2, page 143). The error messages are displayed on dd1 and dd2. The error message is acknowledged by pressing the Enter key (tA4), the parametering mode AdAP is retained, tU is displayed, the defaults can be corrected if necessary. Abortion by the control signals N and ±yBL can be prevented by appropriate connection (locking with controller output AL).

- **Post adaptation**

The data source AdAP is high and may display the end of adaptation when connected for example with L3. The parameters **.o with the ID Pi or Pid and the new parameters **.n with the ID Pi.1 to 8 and Pid.1 to 8 for Pi and Pid controller design are offered. The digits after the Pi or Pid ID indicate the line order.

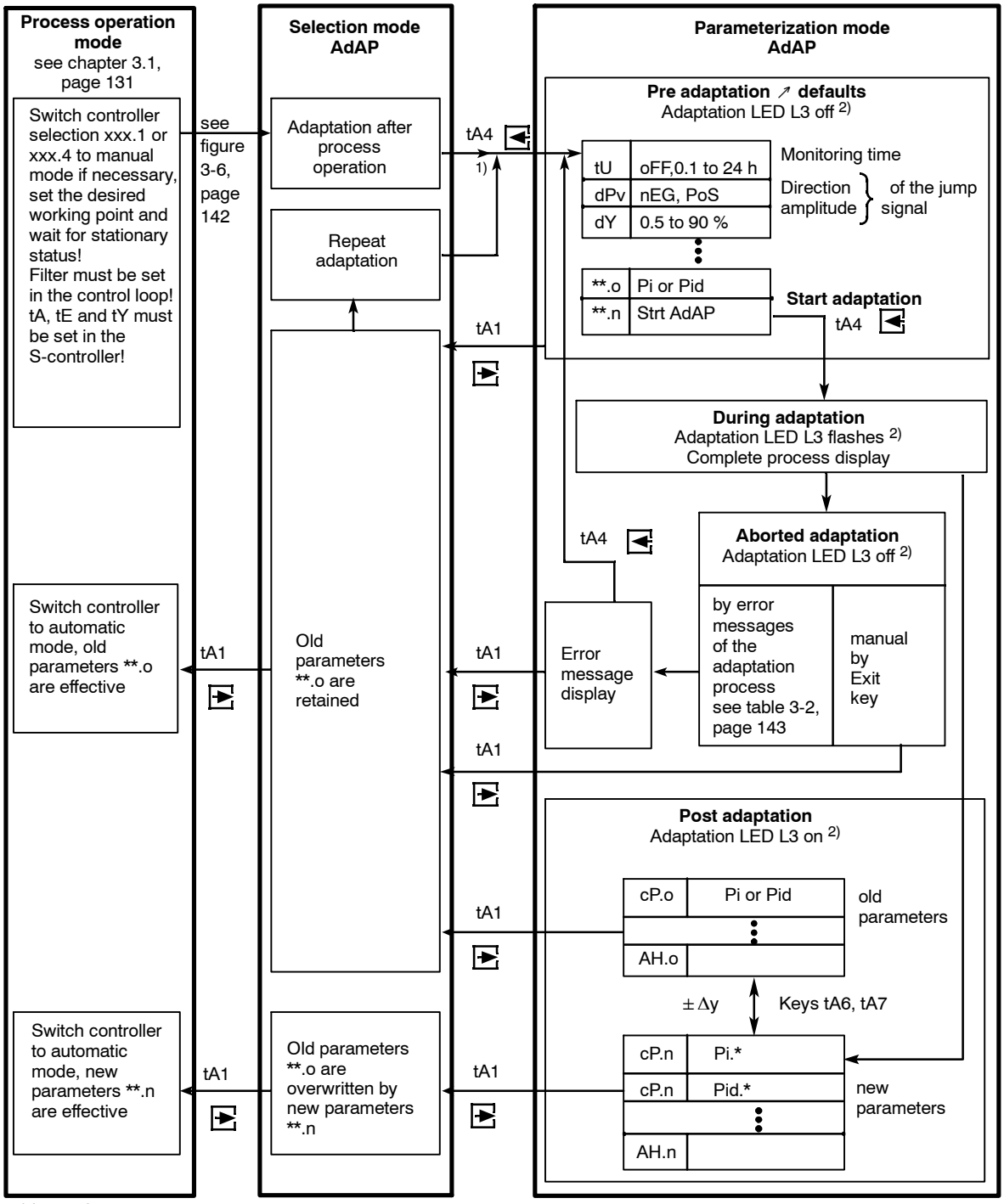
The old and the new parameters are adjustable.

On pressing the Exit key (tA1) the parameters **.o or **.n which have just been selected are transfered to AdAP when returning to the parameter preselection mode. The data source AdAP is now set to low. When transfering **.o, these parameters remain unchanged if they have not been changed manually. When transfering **.n the old parameters are overwritten by the new

parameters. After returning to the parameterization mode AdAP the **.n parameters are identified by Strt AdAP.

The transfered parameters do not affect the process until the process operation mode has switched to Automatic after pressing the Exit key (tA1).

When controlling the parameters with the appropriate control inputs of the controllers, it is not recommendable to transfer the new parameters directly because the function generators following the controlling variable need to be set accordingly. In this case the new parameters must be noted in pairs to the controlling variable to set the function transmitter accordingly. The controlling variable must be displayed during adaptation. To do this use the controller output AL (adaptation in progress) and switch a display over to the controlling variable during adaptation if necessary.



* line order 1 to 8
** parameter name

1) Enter function only active in manual mode
xxx = Ccn K-controller
CSi S-controller internal
CSE S-controller external
} according to FdEF

2) If L3 is wired to the source AdAP.

Figure 3-5 Parameterization mode AdAP

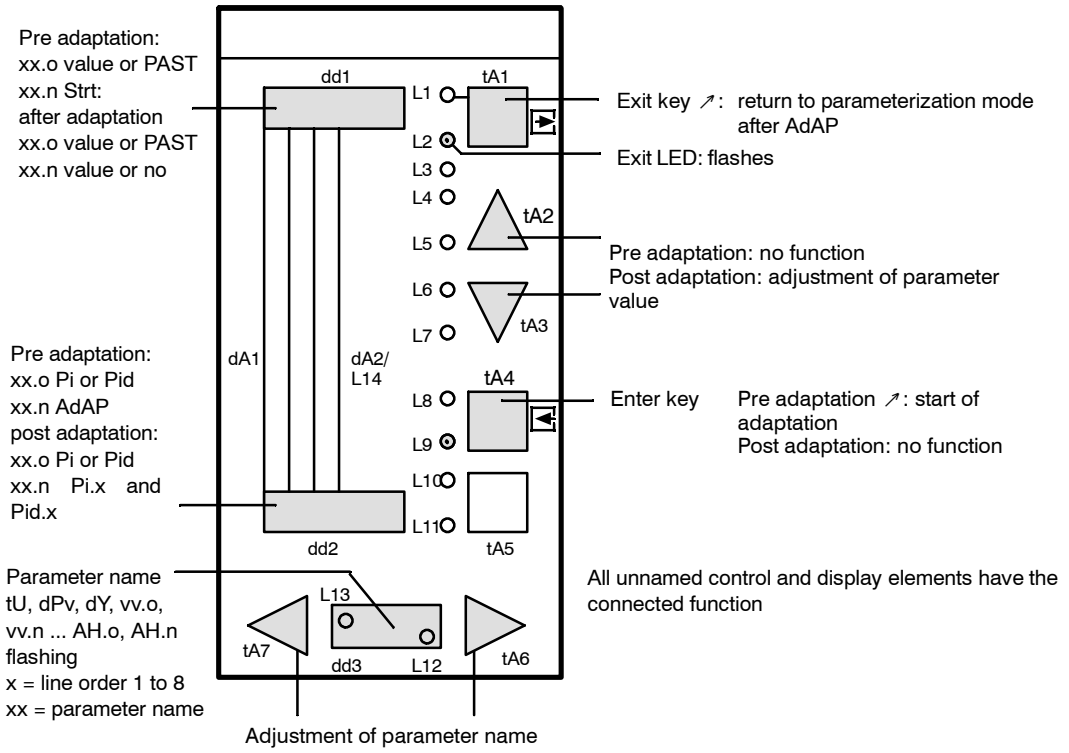


Figure 3-6 Control and display elements before and after adaptation in the parameterization mode AdAP

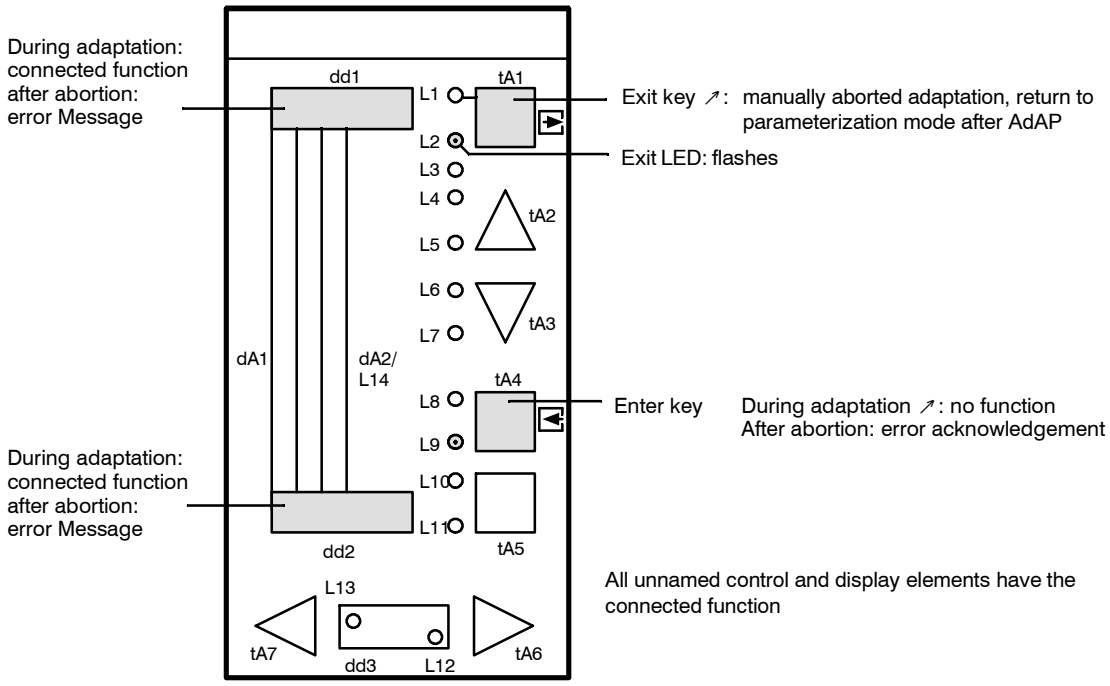


Figure 3-7 Control and display elements during and at abortion of adaptation in the parameterization mode AdAP

• Adaptation error messages

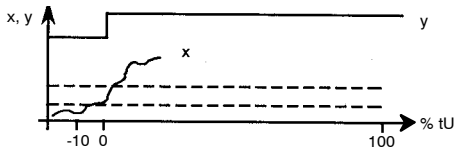
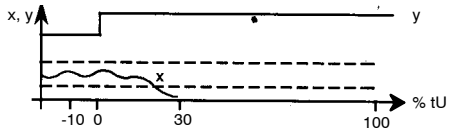
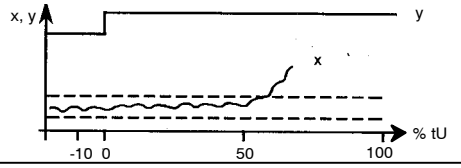
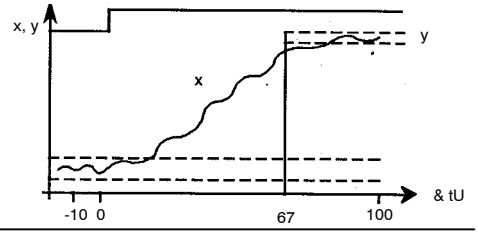
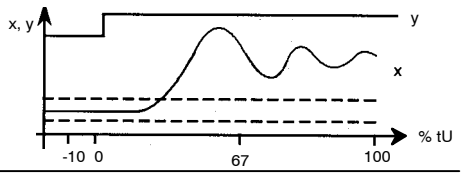
Error message dd1 dd2	Explanation		
not StAt	not stable at 10 % tU after start of adaptation ⇒ wait and restart adaptation		
no dY	after expiry of Ty the y step has not been performed correctly for the S-controller	⇒	Check position feedback and drive of the final control element
Y oFL	y outside the measuring span of 0 to 100%	⇒	$y_{Manual} \pm \Delta y$ too big or too small
ALL PASS	step response in wrong direction within 30 % tU ⇒ Change active direction of the controller ⇒ control loop undershoot (all pass loop), all–pass loops not defined among loop models		
too SMAL	x after 50 % tU still within starting band ⇒ tU too short ⇒ y step too small		
no End	at 67 % tU full scale value not reached ⇒ tU too short ⇒ loop cannot reach full scale value, e.g. integrally active line ⇒ transient recovery time $t_{95} > 12$ h		
Pv oFL	x outside the measuring span 0 to 100 %	⇒	$y_{Manual} \pm \Delta y$ too big or too small
too FAST	because of too small a line time constant accurate adaptation not possible		(transient recovery time $t_{95} < 5$ s)
ovEr Shot	> 10 % overshoot of the transient function ⇒ accurate adaptation not possible		
n MoDE	Tracking mode via the control signals	⇒	cancel mode of operation
YbL MoDE	direction–dependent blocking operation via the control signals	⇒	
no MAnual	exit manual mode during adaptation	⇒	

Table 3-2 Adaptation error messages

Pre adaptation

dd3	dd1 Setting/ display range	dd2	Factory setting	Resolu-tion	Dimen-sion	Parameter meaning/Comments	
tU dPv dY	oFF*), 0.1 - 24.0 nEG, PoS 0.5 - 90.0	Control-led vari-able x	oFF PoS 0.5	0.1 – 0.1	h – %	Monitoring period Direction of step Amplitude of step	Preset. for the adaptation
vv.o	0.100 - 10.00 1)	Pi or Pid	5.000	128 values per octave	1	previous derivative action at:	Tv = oFF Tv ≠ oFF
vv.n	Strt 1)	AdAP	–	–	–	Start of adaptation	
cP.o	0.100 – 100.0 1)	Pi or Pid	0.100	128 values per octave	1	previous proportional gain at :	Tv = oFF Tv ≠ oFF
cP.n	Strt 1)	AdAP	–	–	–	Start of adaptation	
tn.o	1.000 - 9984 1)	Pi or Pid	9984	128 values per octave	s	previous integral reset at:	Tv = oFF Tv ≠ oFF
tn.n	Strt 1)	AdAP	–	–	–	Start of adaptation	
tv.o	oFF 1) 1.000 - 2992 1)	Pi or Pid	oFF	128 values per octave	s	previous derivative action time at:	Tv = oFF
tv.n	Strt 1)	AdAP	–	–	–	Start of adaptation	
AH.o	0.0 - 10.0 1)	Pi or Pid	0.0	0.1	0.1	previous response threshold	
AH.n	Strt 1)	AdAP	–	–	–	Start of adaptation	

1) not adjustable

*) at Tu = oFF the monitoring period is 24 hrs

Post adaptation

dd3	dd1 Setting/ display range	dd2	Factory setting	Resolu-tion	Dimen-sion	Parameter meaning/Comments	
vv.o	0.100 – 10.00	Pi or Pid	5.000	128 values per octave	1	previous derivative action gain at:	Tv = oFF Tv ≠ oFF
vv.n	5.000 0.100 – 10.00	Pid.*)	–	128 values per octave	1	new derivative action gain for	PID-controller
cP.o	0.100 – 100.0	Pi or Pid	0.100	128 values per octave	1	previous proportional gain at:	Tv = oFF Tv ≠ oFF
cP.n 1) cP.n	0.100 – 100.0 0.100 - 100.0	Pi.*) Pid.*)	– –	128 values per octave	1 1	new proportional gain for	PI controller PID controller
tn.o	1.000 - 9984	Pi or Pid	9984	128 values per octave	s	previous integral reset time at:	Tv = oFF Tv ≠ oFF
tn.n tn.n	1.000 - 9984 1.000 - 9984	Pi.*) Pid.*)	– –	128 values per octave	s	new integral reset time for	PI controller PID controller
tv.o	oFF 1.000 – 2992	Pi or Pid	oFF	128 values per octave	s	previous derivative action time at:	Tv = oFF Tv ≠ oFF
tv.n	1.000 – 2992	Pid.*)	–	128 values per octave	s	new derivative action time for	PID-controller
AH.o	0.0 – 10.0	Pi or Pid	0.0	0.1	%	previous response threshold	
AH.n	0.0 – 10.0	Pid	–	0.1	%	new response threshold	

1) step in at cPn after adaptation

*) control loop order 1 to 8

Table 3-3 Adaptation parameter list in parameterization mode AdAP

3.3.3 Configuring Mode oFPA (Offline Parameters)

In the oFPA configuring mode the parameters are arranged whose effect on the process does not need to be monitored when they are adjusted. The other parameters are arranged in the parameterization mode onPA and in the configuring mode CLPA. The offline parameters are listed in table 3-4. The parameters against a white background (signal range or display range of the displays dA1 and dd1 to dd3 are always accessible).

The parameters against a gray background are the private parameters of the complex functions and the signal range of the analog display dA2 as well as the private parameters of the SES. They only appear if the complex functions are defined in FdEF and selected in hdEF dA2 or the SES was answered with YES.

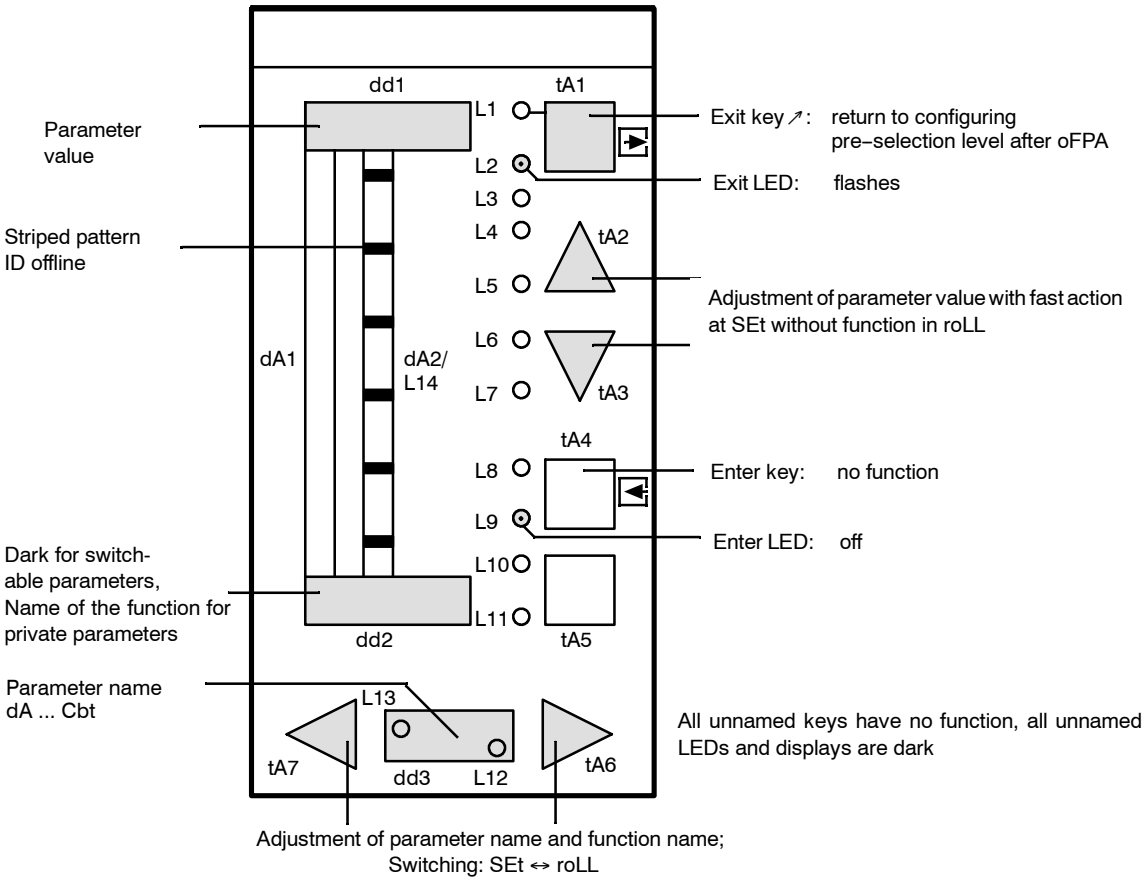


Figure 3-8 Control and display elements in the configuring mode oFPA

dd2	dd3	dd1 Setting range	Factoy setting	Resolu-tion	Di-men-sion	Parameter meaning
dA1.1	dA		0.0			Analog display 1 Input 1 Start of scale } Signal
	dE		100.0			Full scale } range
dA1.2	dA	–199.9 to 199.9	0.0	0.1	%	Analog display 1 Input 2 Start of scale } Signal
	dE		100.0			Full scale } range
dA1.3	dA		0.0			Analog display 1 Input 3 Start of scale } Signal
	dE		100.0			Full scale } range
dA1.4	dA	–199.9 to 199.9	0.0	0.1	%	Analog display 1 Input 4 Start of scale } Signal
	dE		100.0			Full scale } range
dd1.1	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 1 Start of scale }
	dE	-1999 to 19999	100.0			Full scale }
dd1.2	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 2 Start of scale } Display
	dE	-1999 to 19999	100.0			Full scale } range
dd1.3	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 3 Start of scale }
	dE	-1999 to 19999	100.0			Full scale }
dd1.4	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 4 Start of scale } Display
	dE	-1999 to 19999	100.0			Full scale } range
dd2.1	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 1 Start of scale }
	dE	-1999 to 19999	100.0			Full scale }
dd2.2	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 2 Start of scale } Display
	dE	-1999 to 19999	100.0			Full scale } range
dd2.3	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 3 Start of scale }
	dE	-1999 to 19999	100.0			Full scale }
dd2.4	dP	_.––– to _ _ _ _	_ _ _.–	1 digit	–	Decimal point
	dA	-1999 to 19999	0.0		–	Digital display 1 Input 4 Start of scale } Display
	dE	-1999 to 19999	100.0			Full scale } range
dd3.1	dP	_ _.– to _ _ _	_ _ _	1 digit	–	Decimal point
	dA	-199 to 999	0		–	Digital display 3 Input 1 Start of scale }
	dE	-199 to 999	100			Full scale }
dd3.2	dP	_ _.– to _ _ _	_ _ _	1 digit	–	Decimal point
	dA	-199 to 999	0		–	Digital display 3 Input 2 Start of scale } Display
	dE	-199 to 999	100			Full scale } range
dd3.3	dP	_ _.– to _ _ _	_ _ _	1 digit	–	Decimal point
	dA	-199 to 999	0		–	Digital display 3 Input 3 Start of scale }
	dE	-199 to 999	00			Full scale }
dd3.4	dP	_ _.– to _ _ _	_ _ _	1 digit		Decimal point
	dA	-199 to 999	0			Digital display 3 Input 4 Start of scale } Display
	dE	-199 to 999	100			Full scale } range
Cnt1	StP	2 to 4	4	1	-	Demultiplexer max. position
						Pressure–temperature correction computer
CPt 1	PA	0.012 to 1.000	1.000	0.001	1	Correction quotient Pressure Start
↓	PE	1.000 to 99.99	1.000	0.001/0.0 1	1	" End
	tA	0.010 to 1.000		0.001	1	" Temperature Start
CPt 2	tE	1.000 to 99.99	1.000	0.001/0.0 1	1	" End

High speed steps
1) omitted if dA-L = L14 is defined in hdEF
2) omitted if SES = no is defined in hdEF
omitted if not defined in FdEF

Table 3-4 Offline parameter list in the configuring mode oFPA

dd2	dd3	dd1 Setting range	Factory setting	Resolution	Dimension	Parameter meaning
dA2.1 [1)]	dA		0.0			Analog display 2 Input 1 Start of scale
	dE		100.0			Full scale } Signal
dA2.2	dA	–199.9 to 199.9	0.0	0.1	%	Analog display 2 Input 2 Start of scale } range
	dE		100.0			Full scale
dA2.3 [1)]	dA		0.0			Analog display 2 Input 3 Start of scale
	dE		100.0			Full scale } Signal
dA2.4	dA	–199.9 to 199.9	0.0	0.1	%	Analog display 2Input 4 Start of scale } range
	dE		100.0			Full scale
FUL1	0		0.0			Function transmitter 1 (linear), vertex at 0 %
↓	20		20,0			20 %
FUL2	40	–199.9 to 199.9	40.0	0.1	%	Function transmitter 2 (linear) 40 %
↓	60		60.0			60 %
FUL3	80		80.0			Function transmitter 3 (linear) 80 %
	100		100.0			100 %
	–10		-10,0			Function transmitter 1 (parabola), vertex at –10 %
FUP1	0		0.0			0 %
↓	10		10.0			10 %
	20		20.0			20 %
FUP2	30		30.0			30 %
	40		40.0			Function transmitter 2 (parabola) 40 %
	50	–199.9 to 199.9	50.0	0.1	%	50 %
	60		60.0			60 %
	70		70.0			70 %
	80		80.0			80 %
	90		90.0			90 %
	100		100.0			100 %
	110		110.0			110 %
MUP1 MUP2	StP	2 to 8	8	1	-	Multiplexer 1 2 Number of switching steps
SES [2)]	bdr	300 600 1200 2400 4800 9600	9600	–	baud	Serial interface baud rate (transmission speed)
	Lrc	norM CMPL	norM	–	–	Longitudinal parity formation ETX normal complement
	LEt	no L Et–L L–Et	no L	–	–	Longitudinal parity position without Lrc with Lrc after ETX with LRC before ETX
	Prt	EvEn odd	EvEn	–	–	vertical parity formation even odd
	Snr	0 to 125	0	–	–	Station number
	Cbt	OFF	oFF	–	–	CB watchdog on SbE1
		1		–	s	
		2		–	s	
		3		–	s	
		4		–	s	
		5		–	s	
		7		–	s	
		10		–	s	
		15		–	s	
		20		–	s	
		30		–	s	

High speeed steps; [1)] omitted if dA-L = L14 is defined in hdEF.

[2)] omitted if SES = no is defined in hdEF; omitted if not defined in FdEF

Table 3– 4 Offline parameter list in the configuring mode oFPA (continued)

3.3.4 Configuring Mode CLPA (Clock Parameters)

All clock parameters are arranged in the structuring mode CLPA. It is only accessible when the complex function CLoc (arithmetic block d0*.F) has been defined in FdEF.

The assignment of the number of intervals per program (parameter CLPr) prescribes the length of the parameter list for the parameters CLti (duration per interval in the respective program) CLA 1/2 (amplitude of the analog outputs at the start/end interval) and CLb1 to 8 (status of the digital outputs in the interval).

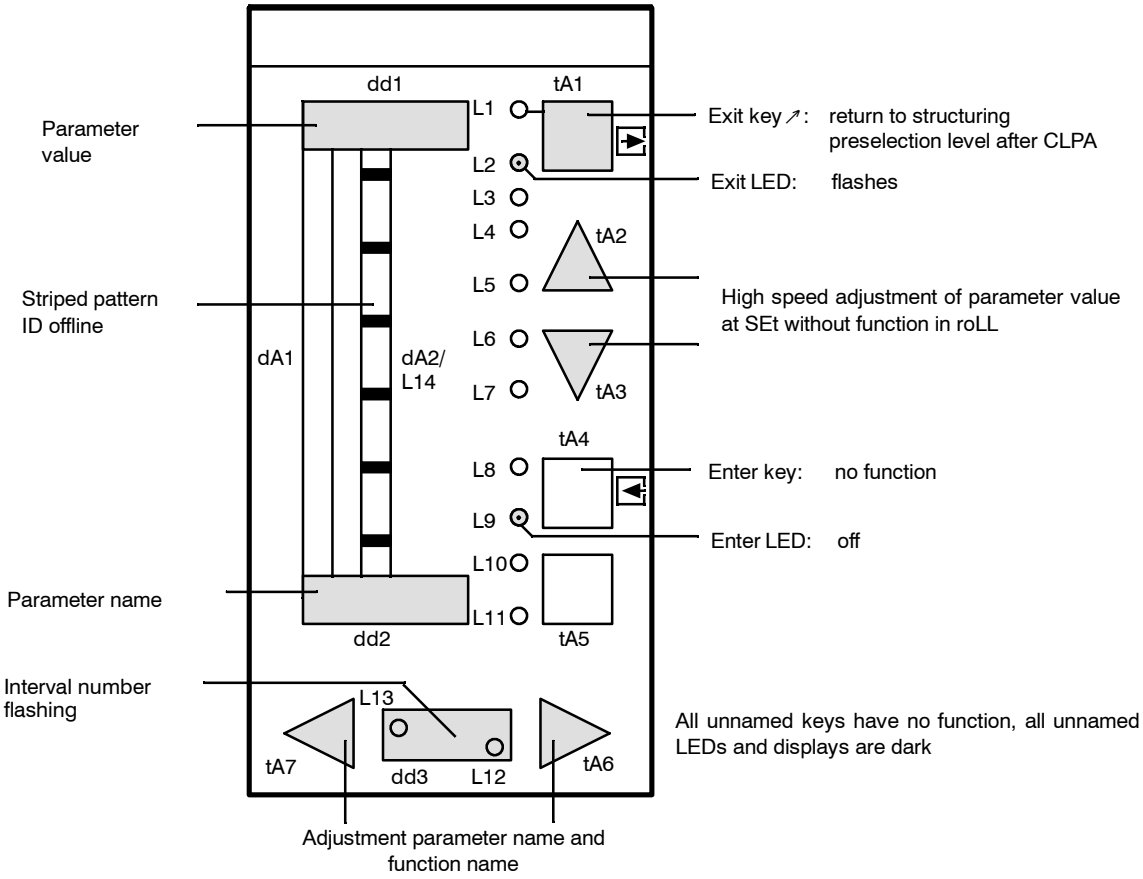


Figure 3-9 Control and display elements in the configuring mode CLPA

dd2	dd3	dd1 Setting range	Factory setting	Resolution	Dimension	Parameter meaning		
CLFo	-	h.,' or ',,,	h, '		h, min min, s	Clock format relative clock		
CLCy	–	CYCL, 1 to 255	CYCL	1	1	Number of program cycles		
CLSb	–	3 6 12 24 60 120 158 360	3		1	Acceleration factor		
CLPr	- -.1 ↓ - -.8	no, 01 to 40	no ↓ no	1	–	Number of intervals per program (total max. 40 intervals for max. 8 possible programs) no = no interval		
CLti	01.1 ↓1) xx.1 ↓ 01.8 ↓1) xx.8	00.01 to 59.59 or 00.01 to 23.59 **depending on CLFo for all programs**	00.01 00.01	1 s 1 min	min, s h, min	Duration per interval in the 1st program Duration per interval in the 8th program		
CLA1	00.1 01.1 ↓1) xx.1	–199.9 to 199.9, nop	0.0	0.1	%	Analog output 1	Amplit. 1st interval start 1st interval end Amplit. last interv. end	in the 1st program
↓	↓	↓	↓	↓	↓			
CLA2	00.8 01.8 ↓1) xx.8		0.0	0.1	%	Analog output 2	Amplit. 1st interval start 1st interval end Amplit. last interv. end	in the 8th program
CLb1	01.1 ↓1) xx.1	Low or High	Lo	-		Digital output 1	Status in the 1st interval Status in the last interval	in the 1st program
↓	↓	↓	↓	↓	↓			
CLb8	01.8 ↓1) xx.8	Low or High	Lo	-		Digital output 8	Status in the 1st interval Status in the last interval	in the 8th program

1) Display according to default in CLPr, xx = last assigned interval number in the respective program

omitted if not defined in FdEF

High speed steps

The structuring mode CLPA can only be selected if the complex function CLoc has been assigned to one of the arithmetic blocks d1 to d3 in FdEF.

Table 3-5 Clock parameter list in the configuring mode CLPA

3.3.5 Configuring Mode hdEF (Define Hardware)

All hardware properties and input and output function properties are combined in a question and answer cycle in the configuring mode hdEF. It is set by setting hardware function (question) in dd2 and hardware selection (answer) in dd1 in pairs. The answers for the properties of the input and output functions specify the length of the lists in the configuring modes oFPA and FCon like FdEF.
The setting becomes valid when switching to the next question or returning to the configuring preselection level after hdEF.

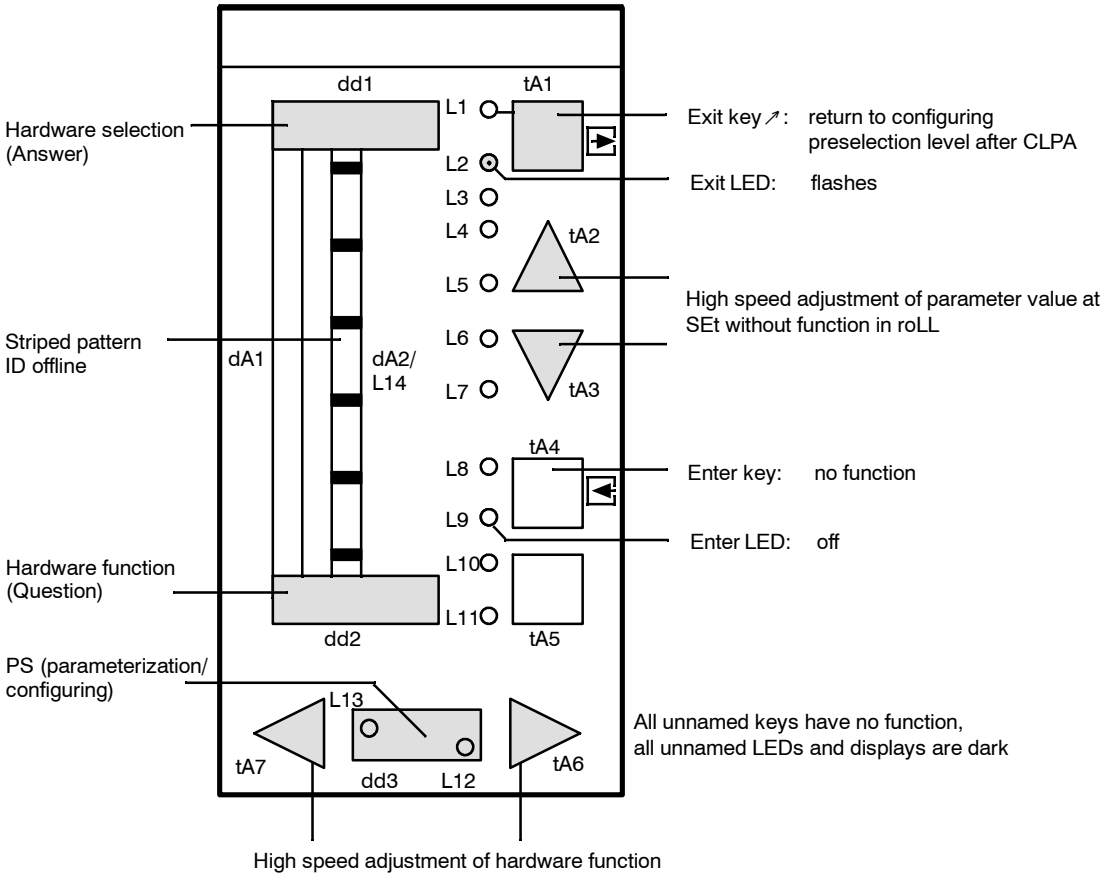


Figure 3-10 Control and display elements in the configuring mode hdEF

Question dd2 Hardware function	Answer dd1 Hardware selection	Factory setting	Meaning
AA1 ↓ AA9	0 MA or 4 MA	0 MA	Signal range analog outputs 0 mA/4 mA
AAU	no or YES	no	Analog output switching
AE1 ↓ AE3	no, 0 MA or 4 MA	no	Signal range analog outputs 0 mA/4 mA
AE4, AE5	no, 0 MA, 4 MA Uni.= Uni._	no	Signal range analog inputs 0 mA/4 mA Uni–module: 0 at sensor failure Uni–module: 1 at sensor failure
AE6 ↓ AE11	no, 0 MA or 4 MA	no	Signal range analog inputs 0 mA/4 mA
AEFr	50 H or 60 H	50 H	Analog inputs mains frequency suppression
bAtt	no or YES	YES	Battery backup RAM (restart conditions)
bAU	no or YES	no	switchover of digital output
dA–L	dA2 or L14	dA2	Display selection analog display or LED
dPon	no or YES	no	Flashing of dd1 to dd3 at Power on
nAME	o1) to 254	0	Name (ID) of user program memory
oP5 ↓ oP6	no 4 bA 5 bE 2rEL 1 AA 3 AE 3 AA	no	Options in slot 5/6 none 4BA24V/2BE 5BE 2BA Relay 1AA y-hold 3AE 3AA/3BE
SES	no or YES no = read only YES = read and write	YES	Serial interface
tA1.U ↓ tA7.U	no, YES or Four	no	Key switching

1) Position 0 cannot be set manually. As soon as the factory setting is changed (parameter or configuring), naME is automatically set to 1. APst sets naME to 0.

= High speed steps

Table 3-6 Hardware function list in the configuring mode hdEF

3.3.6 Configuring Mode FdEF (Define Functions)

Functions required for the user program are defined in the configuring mode FdEF. The functions (answer) are assigned to the initially „empty" arithmetic blocks (question). They are assigned by setting question (arithmetic block) on dd2 and answer (function) on dd1 in pairs. Definition is effected on switching to the next question or returning to the configuring preselection level after FdEF.
Every function assignment to the arithmetic blocks can be overwritten at any time in the configuring mode FdEF or deleted with the assignment ndEF (not defined). The factory setting contains ndEF for all arithmetic blocks.
The defined functions specify the scope of the other configuring modes AdAP, FCon, FPoS, oFPA and CLPA and the scope of the parameterization mode onPA.
A distinction is made between basic functions and complex functions in the definition.

- **Basic functions**

  109 arithmetic blocks b01.F to bh9.F with a max. 3 inputs and one output are available for assignment with the 32 basic functions. The basic functions can be used as often as you like and are offered in the answer cycle only for these arithmetic blocks.

- **Complex functions**

  20 arithmetic blocks with different input/output formats are available for the assignment with the 20 complex functions.

33	Arithmetic blocks c01.F to c33.F with 4 inputs 1 output	for	AFi1/2, Ain1 to 4, bin1 to 6, CPt1/2, dti1/2, FUL1 to 3, FUP1/2 PUM 1 to 4, SPR1 to 8
4	Arithmetic blocks d01. F to d04. F with 12 inputs 14 outputs	for	CLoc, MUP1/2, Cnt1
4	Arithmetic blocks h01. F to h04.F with 18 inputs 4 outputs	for	Ccn1 to 4, CSE1 to 4, CSi1 to 4

  The complex functions are offered in the answer cycle according to the different arithmetic blocks and can be used as often as they are stored.

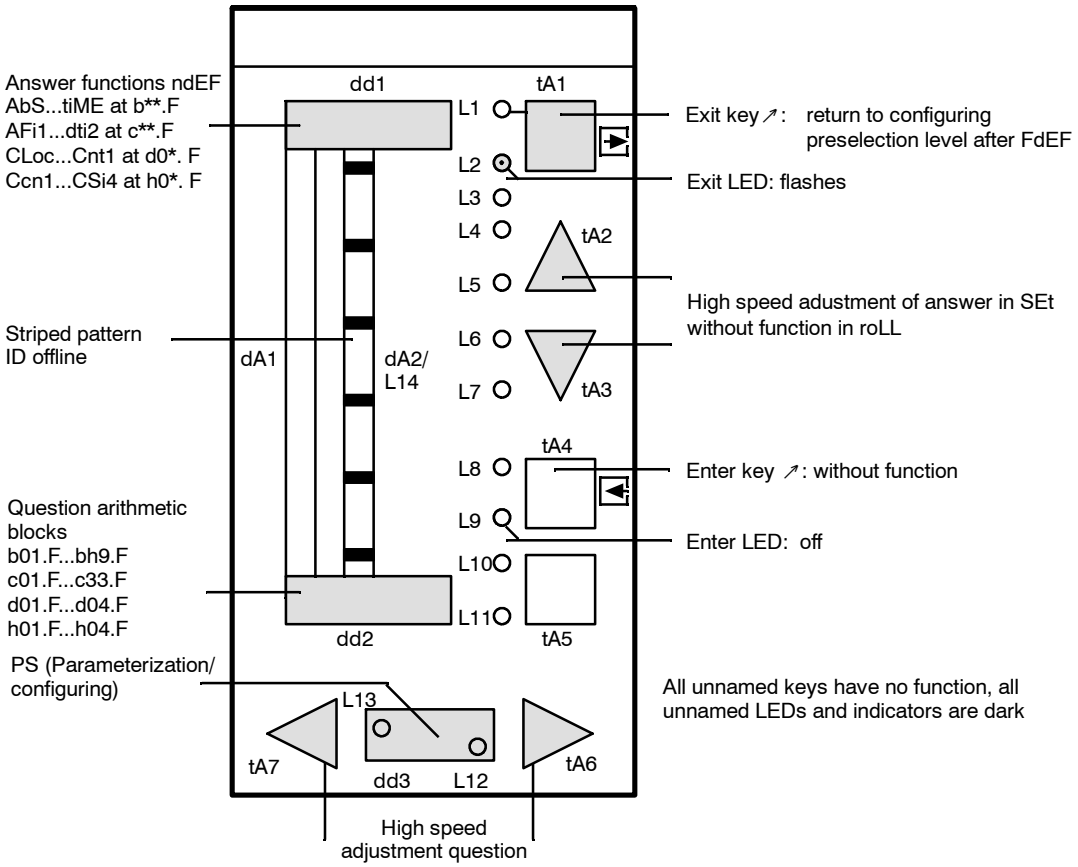


Figure 3-11 Control and display elements in the configuring mode FdEF

Question Arithmetic blocks dd2	Answer Functions dd1
b01.F	ndEF
↓	AbS
b09.F	Add
b10.F	AMEM
↓	AMPL
b19.F	And
b20.F	ASo
↓	bSo
b29.F	CoMP
b30.F	CoUn
↓	dEbA
b39.F	dFF
b40.F	diF
↓	div
b49.F	Eor
b50.F	Filt
↓	LG
b59.F	LiMi
b60.F	LinE
↓	Ln
b69.F	MAME
b70.F	MASE
↓	MIME
b79.F	MISE
b80.F	MULt
↓	nAnd
b89.F	nor
b90.F	or
↓	Pot
b99.F	root
bh0.F	SUb
↓	tFF
bh9.F	tiME

Question Arithmetic blocks dd2	Answer functions dd1
c01.F	ndEF
↓	AFi1
c09.F	AFi2
c10.F	Ain1
↓	↓
c19.F	Ain4
c20.F	bin1
↓	↓
c29.F	bin6
c30.F	CPt1
↓	CPt2
c33.F	dti1
	dti2
	FUL1
	FUL2
	FUL3
	FUP1
	FUP2
	SPr1
	↓
	Spr8
	PUM1
	↓
	PUM4
d01.F	ndEF
d02.F	CLoc
d03.F	MUP1
d04.F	MUP2
	Cnt1
h01.F	ndEF
h02.F	Ccn1
h03.F	Ccn2
h04.F	Ccn3
	Ccn4
	CSE1
	CSE2
	CSE3
	CSE4
	CSi1
	CSi2
	CSi3
	CSi4

High speed steps

Table 3-7 Question/answer cycle in the configuring mode FdeF

3.3.7 Configuring Mode FCon (Switch Functions, Connection)

In the FCon configuring mode all the functions defined in FdEF are connected with each other and with the inputs or outputs of the output or input functions (software connection). A connection is established by setting a paired data source (outputs)/data sink (inputs) in dd1/dd2. First the data source (question) and then the corresponding data sink (answer) is set. The connection is established on switching to the next question or returning to the configuring preselection mode after FCon.

If controllers CSE* or CSi* were assigned to the **arithmetic blocks h01.F** in FdEF, the outputs of the S-controllers h1.2A (+Δy) or h1.3A (–Δy)are permanently assigned to the question positions bA05 and bA06, adjustment is not possible.

If controllers CSE* or CSi* were assigned to the **arithmetic blocks h02.F** in FdEF, the outputs of the S-controllers h2.2A ($\pm\Delta$y) or h2.3A (–Δy)are permanently assigned to the question positions bA07 and bA08, adjustment is not possible.

If the controllers CSE* or CSi were assigned to the **arithmetic blocks h03.F** in FdEF, the outputs of the S-controllers h3.2A (+Δy) or h3.3A (–Δy) are permanently assigned to the question positions bA3.1/bA3.2 and bA4.1/bA4.2, adjustment is not possible.

If the controllers CSE* or CSi* were assigned to the **arithmetic blocks h04.F** in FdEF, the outputs of the S-controllers h4.2A ($\pm\Delta$y) or h4.3A (–Δy) are permanently assigned to the question positions bA1.1/bA1.2 and bA2.1/bA2.2, adjustment is not possible.

The data sinks and sources of the arithmetic blocks not defined in FdEF and the input and output functions identified by no in hdEF and the SES are faded out of the answer cycle.

Since only combinations of the same signal types (only analog or only digital) are allowed as question (sink) and answer (source) pairs, only the corresponding data sources can be set on dd1 in the answer cycle. This supresses illogical connections.

Every data sink can only be assigned one data source, whereas every source can be connected with as many sinks as you like. The parallel loop of inputs (sinks) is therefore achieved by connection of the respective inputs with the same output (source). The defaults of the inputs (Hi, Lo, ncon or numeric values) are transferred to the Fcon mode in the description and can be changed (overwritten) there if necessary.

- **Reactions in FCon if changes have been made in FdEF or hdEF**

  - Deleting a function with ndEF or no:

    The existing connection to the inputs and outputs of the deleted function block is removed and inputs of the other function blocks fed by the output or the outputs of the deleted function block are identified by ncon.

- Overwriting with another function (or YES in hdEF)

  The existng connection to the inputs and outputs of the changed arithmetic block is removed. The inputs of the redefined function block are occupied by the default of the newly defined function. The inputs of the other function blocks previously fed by the outputs of this function block are identified by ncon.

- **Error message ncon Err**

  It is also permissible to terminate the connection with data sinks identified by ncon. However, it is advisable to add the missing connections because the desired functions cannot run with undefined inputs.

  See chapter 1.5.6, page 38 ”Error message” for details!

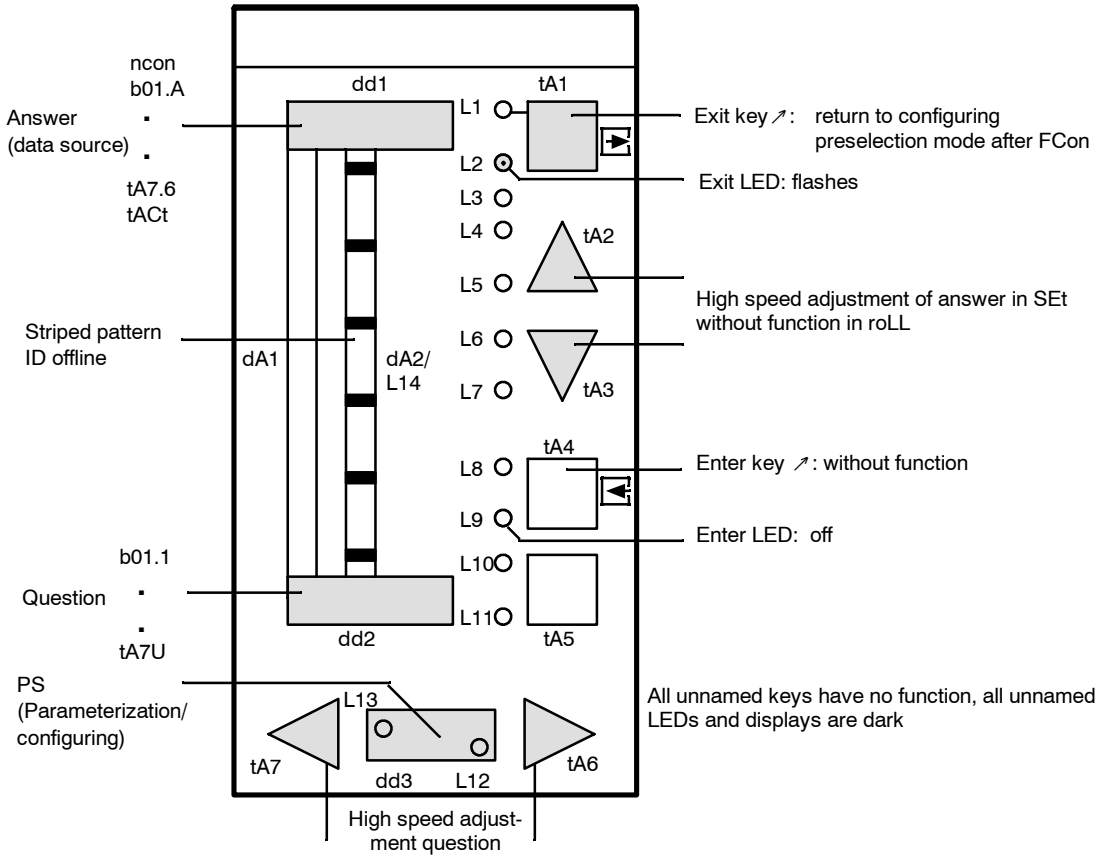


Figure 3-12 Control and display elements in the configuring mode FCon

Question data sinks in dd2

Arithmetic blocks		Output range	
b01.1	h1.01	AA1.1	dd1.M
b01.2	↓	AA1.2	dd1.U
b01.3	h1.18	↓	↓
↓	h2.01	AA4.1	dd3.1
b09.1	↓	AA4.2	dd3.2
b09.2	h2.18	AA05	dd3.3
b09.3	h3.01	↓	dd3.4
b10.1	↓	AA09	dd3.M
↓	h3.18	AAU	dd3.U
bh9.3	h4.01	bA1.1	L01.1
c01.1	↓	bA1.2	L01.2
c01.2	h4.18	↓	L01.3
c01.3		bA4.1	L01.4
c01.4		bA4.2	L01.M
↓		bA05	L01–U
c09.1		bA06	↓
c09.2		bA07	L13.1
c09.3		bA08	L13.2
c09.4		bA09	L13.3
c10.1		↓	L13.4
c10.2		bA16	L13.M
c10.3		bAU	L13.U
c10.4		bLb [1]	L14.0
↓		bLPS [1]	↓
c33.1		bLS [1]	L14.9
c33.2		dA1.1	SAA1
c33.3		dA1.2	↓
c33.4		dA1.3	SA16
d1.01		dA1.4	SA(E)1.1
↓		dA1.M	SA(E)1.2
d1.12		dA1.U	↓
d2.01		dA2.1	S(E)16.1
↓		dA2.2	S(E)16.2
d2.12		dA2.3	SbA1
d3.01		dA2.4	↓
↓		dA2.M	Sb16
d3.12		dA2.U	tA1M
d4.01		dd1.1	tA1U
↓		dd1.2	↓
d4.12		dd1.3	tA7U
		dd1.4	

High speed steps

omitted if not assigned in hdEF

Question and answer positions of the arithmetic blocks only appear if functions have been assigned to the arithmetic blocks in FdEF.
Only analog or digital positions respectively appear for analog and digital question positions.

[1] bLb, bLPS and bLS are only connectable as sinks with Lo, bE01 to bE14, the SES sources SbE1 to SbE8 and ncon. If the CB watchdog responds, the SES sources linked with bLPS or bLS are set to Lo so that the parameterization and configuring levels remain accessible (even when no SES access is possible). The same procedure also runs in the SES parameter setting Cbt = oFF.

Table 3-8 Question/answer cycle in the configuring mode FCon

Answer data sources in dd1		
Arithmetic blocks analog/digital	Input and output range	
	analog	digital
b01.A	AA1.3	AdAP
b02.A	AA2.3	AE1ϟ
↓	AA3.3	↓
bh8.A	AA4.3	A11ϟ
bh9.A	AE1A	bA1.3
c01.A	↓	bA2.3
c02.A	AE11	bA3.3
↓	PD01	bA4.3
c33.A	↓	bE01
d1.1A	PD40	↓
↓	PL01	bE14
d1.14	↓	Hi
d2.1A	PL40	Lo
↓	SA1.3	nAEϟ
d4.14	↓	nPar
h1.1A	S16.3	nPon
↓	–1.000	nStr
h1.4A	–0.500	oPEr
h2.1A	–0.200	rES1
↓	–0.100	rES2
h4.4A	–0.050	SbE1
	–0.020	↓
	–0.010	SbE9
	–0.005	SbF0
	–0.000	↓
	0.001	SbF6
	0.002	tA1.1
	0.005	tA1.2
	0.010	tA1.3
	0.020	tA1.4
	0.050	tA1.5
	0.100	tA1.A
	0.200	tA1.b
	0.500	tA1.c
	1.000	tA1.d
	1.050	tA1.E
	1.100	tA1.F
	1.050	tA2.1
	1.100	↓
	2.718	tA7.F
		tAC1
		tAC2
		tACt

High speed steps

Question and answer positions of the arithmetic blocks only appear if functions have been assigned to the arithmetic blocks in FdEF.

Only analog or digital answer positions respectively appear for analog and digital question positions.

omitted if not assigned in hdEF

Table 3-8 Question/answer cycle in configuring mode FCon (continued)

3.3.8 Configuring Mode FPoS (Position Functions)

Time processing of the functions defined in FdEF is determined in the FPoS mode. Time processing of the functions is inserted chronologically correctly between the input and output functions. Positioning is effected by setting a pairing positioning number (question) in dd2 and arithmetic block (answer) in dd1 and becomes valid on switching to the next question or when returning to the configuring preselection mode after FPos.

Only defined functions appear in the answer cycle, already positioned functions are automatically deleted from the answer cycle.

When positioning, the guideline applies that the input variables of a function must already have been calculated before the function is are processed. Since this requirement cannot be met, it must be taken into account that values from the previous cycle are used for operation in the case of feedbacks.

- **Reactions in FPoS, if a change has been made in FdEF**

  - Deleting a function with ndEF
    The arithmetic block is deleted from the positioning sequence. The processing order of the remaining arithmetic blocks stays the same. The gap is closed automatically by shifting together (auto–delete).
  - Overwriting the arithmetic blocks with another function
    The time positioning remains the same

  Existing positioning sequences can be corrected with inSt, dElt and nPos (in the answer cycle).

- **Function inSt (insert)**

  To insert a not yet positioned function in an existing positioning sequence.

  Set the position number with tA6/7 instead of which the not yet positioned function block is to be inserted. Set inSt with tA2/3, the Enter LED flashes and indicates that the Enter key is active.
  On pressing the Enter key tA4 the set position number nr** is indicated with nPoS and the Enter LED goes out.
  The previous positioning sequence is shifted up one position from nr**, the nr** can now be overwritten with the still free function. If the end of the positioning sequence is reached by the inSt function, the function cannot be executed (Enter LED does not go out).

- **Function dELt (delete)**

  To close nPoS-gaps within a positioning sequence. Set the position number to be deleted with tA6/7. Set dELt with tA2/3, the Enter LED flashes and indicates that Enter key tA4 is active. On pressing the Enter key the set position number nr** is identified with the function of the following position number. The previous positioning sequence is moved down one position number from nr**. When all defined functions have been positioned, the dELt function is only offered at positions with assigned nPoS.

- **Function nPoS (not positioned)**

  To exchange function blocks within a positioning sequence. Select the position numbers to be exchanged with tA6/7 and assign nPoS respectively with tA2/3. Then the functions overwritten with nPoS are available again in the answer cycle. They can be assigned to the position numbers occupied with nPoS.

- **Error messages**

  - **–PoS Err**
  - **nPoS Err**
    Error description and correction see chapter 1.5.6, page 38.

Note

Both error messages are only of an informative nature. If the error is not corrected, the user program is only processed up to the first position number identified by nPoS. In this way it is possible to test longer programs in sections. Displays and LEDs may have to be wired with the outputs of the last processed function blocks.

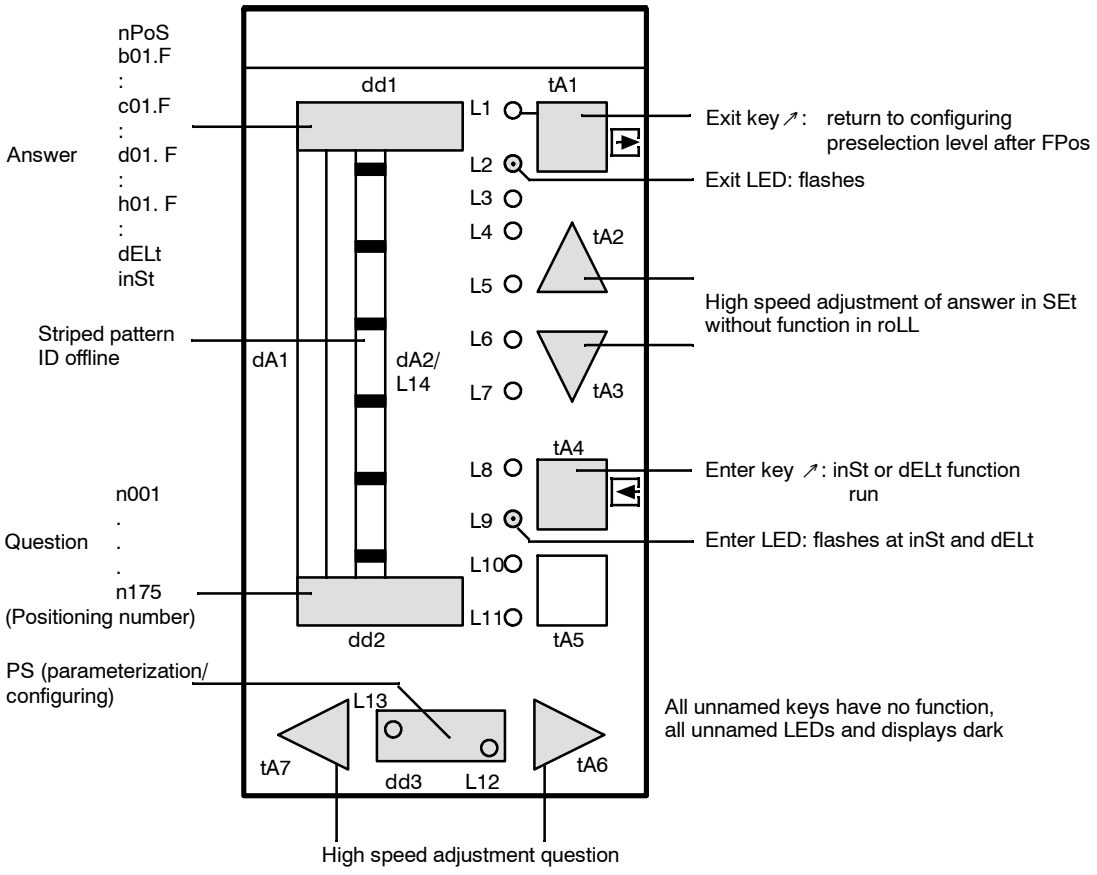


Figure 3-13 Control and display elements in the configuring mode FPoS

Question Positioning no. dd2	Answer Arithmetic block dd1
n001	nPoS
↓	b01.F
n009	↓
n010	b09.F
↓	b10.F
n019	↓
n020	b19.F
↓	↓
n029	bh0.F
n030	↓
↓	bh9.F
n099	c01.F
n100	↓
↓	c09.F
n109	c10.F
↓	↓
n170	c33.F
↓	d01.F
n175	↓
	d04.F
	h01.F
	↓
	h04.F
	dELt[1)]
	inSt [2)]

1) delete only effective with Enter key
2) insert only effective with Enter key

High speed steps

Answer cycle: Arithmetic blocks marked by ndEF in FdEF do not appear

Table 3-9 Question/answer cycle in the configuring mode FPoS

3.3.9 Configuring Mode APSt (All Preset, Factory Setting)

The configuring mode APSt serves to reset **all** device functions (parameters and structures) to the **factory setting**. We recommend you to run the APSt function first if major changes are to be made to the configuration.

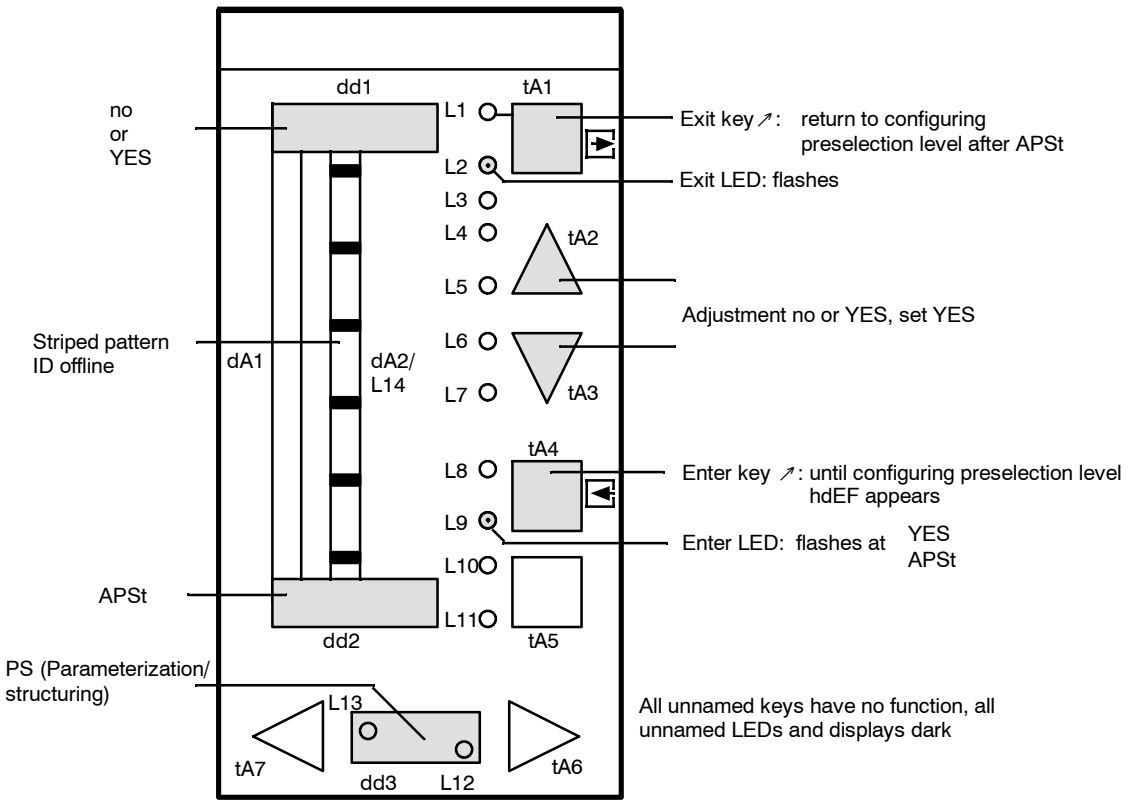


Figure 3-14 Control and display elements in the configuring mode APSt

No APSt appears after jumping to the configuring mode APSt with the Enter key. Set YES with tA2 and press the Enter key tA4 until the configuring preselection mode with hdEF appears. The Preset function is run. Select configuring mode hdEF by pressing the Enter key and re-structure the device. The application program or factory setting are not stored until the process operation level is reached.

- **Error message APSt MEM**

  If the process operation level is switched to after the APSt function or a Power on or Hard reset takes place in a SIPART DR24 with factory setting, the flashing error message APSt MEM appears in dd1 and dd2. It is possible to switch to the parameterization preselection mode with key tA5.

3.3.10 Configuring Mode CAE4/CAE5 – Setting UNI Module(s)

The measuring ranges for the various selectable signal transmitters for slot 2 (AE4) or slot 3 (AE5) can be defined in these menus and fine adjustment performed if necessary.

The CAE4 menu is only offered in the selection level if AEF is set at uni._ or uni.¯ in the configuring mode hdEF.

The CAE5 module is only offered in the selection level if AE5 is set to uni._ or uni.¯ in the configuring mode hdEF.

In the uni._ selection the corresponding measuring signal is set to 0 in the event of a sensor failure, in uni.¯ selection to 1.

An error message will appear if the UNI module is not available: OP.. / 2,3..

The following parameters are available in the CAE4/CAE5 menus for setting the measuring range and adjustment:

Display dd2 parameter	Parameter meaning	Display dd1 Parameter range	Meaning of parameter	Factory setting	Display unit	Display/function only at:
SEnS	Sensor type	Mv. tc.in tc.EH Pt.4L Pt.3L Pt.2L r.– r.¯	Mv signal Thermocouple internal reference point Thermocouple external Reference point PT100 4–wire PT100 3–wire PT100 2–wire Resistor < 600 Ω Resistor < 2.8 kΩ	Mv.		
unit	Temperature unit	°C °F °AbS	Degrees Celsius Degrees Fahrenheit Degrees Kelvin	°C		
tc	Thermocouple type	L,J,H,S,b,r,E n,t,U Lin	Type L,J,K,S,B,R,E,N,T,U Any type (without linearization)	L		SEnS=tc.in, tc/EH
tb [1]	Temperature reference point	0.0...400.0		50.0	°C, °F, °AbS	SEnS=tc.EH
Mr	Line resistance	0.00...100.00		10.00	ohms	SEnS=Pt.2L
Cr	Calibration line resistance	Difference to Mr			ohms	SEnS=Pt.2L
MP	Decimal point measuring range	_.––– to ____		___.–		
MA [2]	Range start	–1999...19999		0.0	Mv, °C, °F, °AbS	
ME [2]	Range end	–1999...19999		100.0	depending on setting SEnS	
CA [3]	Calibration range start	curr. measured value +/– ΔA				
CE [3]	Calibration range end	curr. measured value +/– ΔE				
PC [4]	Preset calibration	no,YES,no C				SEnSE!=r._, r.¯

1) If no specified type of thermocouple is selected with tc=Lin, parameter tb is inactive.
2) The set range normalizes the measured value to 0 to 1 for transfer to the switchable range. If the physical operating display of the measuring value is to be made, the assigned display dd, dA, dE must be set accordingly.
3) For SEnS=r._/r.¯ the unit of the CA/CE display is in %.
4) Effect PC for SEnS = Mv., tc.in, tc.EH, Pt.2L, Pt.3L, Pt.4L.
PC=no C is displayed with A=E=0. It is not possible to switch to "YES" with tA2.
PC=no is displayed by adjusting CA/CE (fine calibration). It is possible to switch to "YES".
Fine calibration is reset by pressing the Enter key (3s). (ΔA=ΔE=0, PC=no C).

The corresponding settings of the CAE4(5) menus for the different signal transmitters are described below.

The range and thus the current measured value can be corrected with the parameters CA/CE to compensate tolerances of the transmitters or adjustments with other display instruments.

3.3.10.1 Measuring Range for mV (SEnS=Mv.)

- **MA/ME measuring range**

  Call parameters MA, ME, set range start and end:
  −175 mV ≤ MA ≤ ME +175 °C

- **CA/CE fine adjustment**

  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.2 Measuring Range for U, I (SEnS=Mv.)

- **MA/ME range**

  The setting is made in mV (−175 mV to +175 mV);
  The input signal types U and I are set to range 0/20 to 100 mV in the measuring range plug (6DR2805−8J);

  Example: 0 to 10 V or 0 to 20 mA: MA = 0, ME = 100;
  2 to 10 V or 4 to 20 mA: MA = 20, ME = 100

  Call parameters MA, ME, set range start and end:

- **CA/CE fine adjustment**

  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.3 Measuring Range for Thermocouple with Internal Reference Point (SEnS=tc.in)

- **Set tc thermocouple type**
- **MA/ME range**
  Call parameters MA, ME, set range start and end according to the temperature unit (unit).
- **CA/CE fine adjustment**
  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.4 Measuring Range for Thermocouple with External Reference Point (SEnS=tc.EH)

- **Set tc thermocouple type**
- **tb–external reference point temperature**
  Set the external reference point temperature with tb. Specify temperature unit with unit.

  Attention: tb has no effect at tc=Lin
- **MA/ME range**
  Call parameters MA, ME, set range start and end according to temperature unit (tc).
- **CA/CE fine adjustment**
  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.5 Measuring Range for PT100–4–wire and PT100–3–wire Connection (SEnS=Pt.3L/PT.4L)

- **MA/ME range**
  Call parameters MA, ME, set range start and end:
  -200 °C ≤ MA ≤ ME +850 °C
  Specify temperature unit with Unit.
- **CA/CE fine adjustment**
  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.6 Measuring Range for PT100–2–wire Connection (SEnS=Pt.2L)

- **MR/CR adjustment of the feed line resistance**

  Path 1: The feed line resistance is known.
  - Enter the known resistance with parameter MR.
  - CR is ignored.

  Path 2: The feed line resistance is unknown.
  - Short circuit PT100 sensor at the measuring site.
  - Call parameter CR and press Enter key until 0.00Ω is displayed.
  - MR displays the measured resistance value.

- **MA/ME measuring range**

  Call parameters MA, ME, set range start and end:
  -200 °C ≤ MA ≤ ME +850 °C
  Specify temperature unit with Unit.

- **CA/CE fine adjustment**

  Call parameter CA:
  Set signal at the low end of the range, correct the display with CA if necessary.

  Call parameter CE:
  Set signal at the top end of the range, correct the display with CE if necessary.

3.3.10.7 Measuring Range for Resistance Transmitter (SEnS=r._ for R < 600 Ω, SEnS=r. ¯ for R< 2.8 kΩ)

Path 1: The start and end values of the R–potentiometer are known.
- Call parameters **MA, ME**, set range start and end:
  0 Ω ≤ MA ≤ ME 600 Ω/2.8 kΩ
- Parameters **CA/CE** display at R=MA 0 %, at R=ME 100 %.

Path 2: The start and end value of the R–potentiometer are unknown.
- Call parameter **CA**:
  Move final control element to position 0%, press Enter until 0.0 % is displayed.
- Call parameter **CE**:
  Move final control element to position 100 %, press Enter until 100.0 % is displayed.
- Parameters **MA/ME** show the appropriate resistance values.
- **MP** must be set so that there is no 'exceeding of the range' (display: oFL)

4 Commissioning

4.1 General Information

The procedure for commissioning and testing depends on the function of the user program *), therefore only general hints can be given here.

Instructions for optimizing the controller function can be found in chapter 1.5.7, page 42, blocks h (controller).

4.2 Test

We recommend you to configure manual setting modes and fully exploit the display possibilities which may only be utilizable for commissioning. We recommend you to proceed section by section for testing a configured user program. This can be achieved by nPoS gaps in the positioning sequence (see chapter 3.3.8, page 159). Displays or analog outputs or LEDs or digital outputs must then be connected in the meantime at the respective end of the section. The necessary measuring results can also be achieved by connecting switching functions of the displays and LEDs which are only activated during the test phase.

To test the SIPART DR24 hardware, simple connections are chosen by connecting inputs and outputs with each other for example and using displays and LEDs for displaying or signaling.

*) No user program is stored when delivered (factory setting)!

5 Maintenance

5.1 General Information and Handling

The controller is maintenance–free. White spirit or industrial alcohol is recommended for cleaning the front foil and the plastic housing if necessary.

In the event of an error the modules

- Front module
- Main board
- Option modules

may be changed freely without readjustment with power supplied.

ATTENTION

All modules contain components which are vulnerable to static. Observe the usual safety precautions!

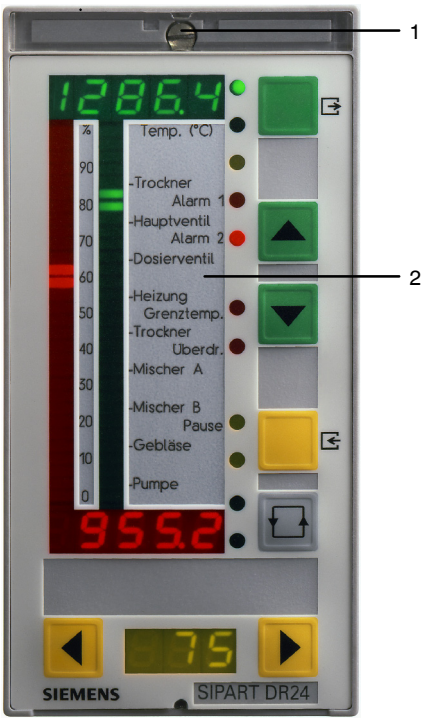
Use y_{hold} modul to maintain the manipulated variable signal on K–controllers (see chapter 1.4.2, page 12). Final control elements on S–controllers remain in their last position.

WARNING

The power supply unit and the interface relay may only be changed when the power supply has been safely disconnected!

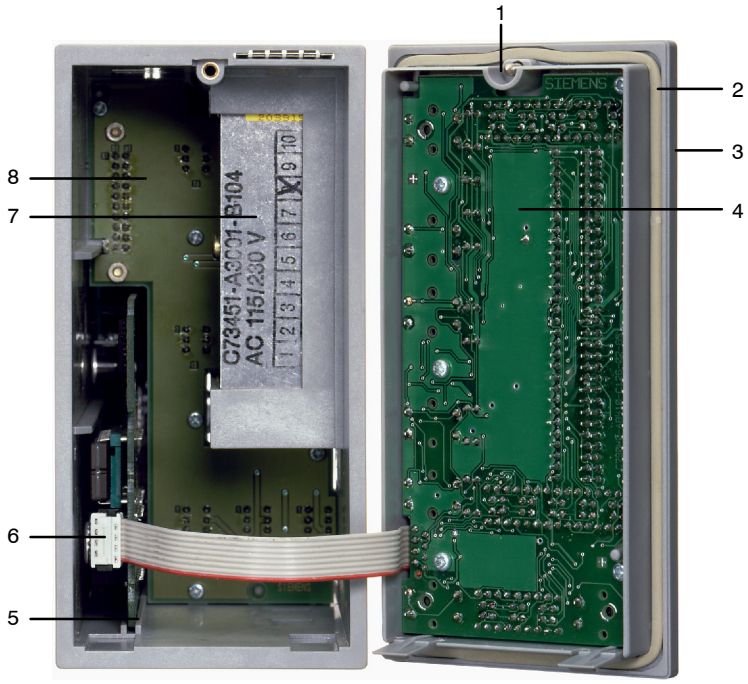
WARNING

Modules may only be repaired in an authorized workshop. This applies in particular for the power supply unit and the interface relay due to the safety functions (isolation and functional extra–low voltages).



1 Fixing screw for the front module
2 Label underneath the front foil (customer foil)

Figure 5-1 Front module with rating plate and cover removed



1 Fixing screw
2 Seal
3 Front panel
4 Front board
5 Main board
6 Ribbon cable
7 Power supply unit
8 Connection plate

Figure 5-2 Controller with front module open

- **Replacing the front module**

  - Carefully lever out the label cover with a screwdriver at the cutout at the top and snap the cover out of the bottom hinge points by bending slightly.
  - Loosen screw (captive) (see (1) Figure 5-1, page 170).
  - Tip the front module at the screw head and pull out to the front angled slightly until the plug of the ribbon cable is accessible.
  - Pull off the plug from the ribbon cable (see (6) Figure 5-2, page 170).
  - Install in reverse order. Make sure the seal is positioned perfectly!

- **Replacing the label**

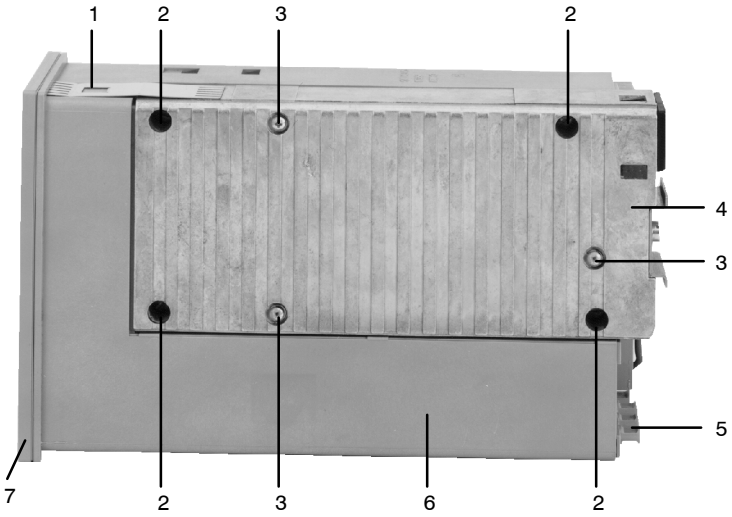
  Pull out the label from beneath the front plate with a pair of tweezers (remove the transparent foil first if necessary). It has a white background on the labelable sections. The surface is suitable for printing with a laser printer.

- **Replacing the main board and option module**

  - Pull out the plug terminal.
  - Release the lock and pull out the module.
    Attention:
    Remove the front module from the main board first (connection cable!)
  - Push in the new module as far as it will go and lock it (the modules are slot–coded but make sure the right modules are plugged into the slots provided for different options).
  - Plug in the terminal (pay attention to slot labeling!).

- **Replacing the power supply unit**

  - Pull out the mains plug!
  - Loosen the clamps and remove the device from the panel.
  - Loosen the four fixing screws of the power supply unit (see (2) Figure 5-3) (**not** the 3 plated Phillips screws (3) Figure 5-3) and pull out the power supply unit in screw direction.
  - Bend the PE conductor contact spring slightly upwards and place the new power supply unit carefully on the plug terminals in screw direction and make sure the guide lugs snap in by moving slightly from side to side (it can no longer be moved from side to side when it has snapped in).
  - Tighten the four fixing screws diagonally.



1 PE conductor contact spring
2 Fixing screws for the power supply unit
3 Plated Phillips screws for fixing the power supply circuit board in the housing
4 Power supply unit
5 Blanking plate
6 Plastic housing
7 Front module

Figure 5-3 Fixing the power supply unit

- **LED test and software state, cycle time**

  If the Shift key (tA5) is pressed for about 10s (after 5 s “PS” appears flashing on dd3), this starts the LED test. All LEDs turn on, the digital displays show “18.8.8.8” or “·8.8.8.” and a light spot from 0 to 100 % consisting of three LEDs runs on the two analog displays (on reaching 100 % the light spot starts again at 0 %).

  If tA1 is also pressed permanently during the lamp test, “dr24” appears on dd1 and the software state of the device appears on dd2 and the cycle time in ms on dd3.

  During the LED test and display of the software state and cycle time, the SIPART DR24 continues to operate online in its last operating mode.

5.2 Spare Parts List

Item	Figure	Description	Comments	Order number
1		**Front module**		
1.1	(7) Figure 5-3	Front module complete	without rating plate label	C73451-A3001-D41
1.2	–	Front frame with foil		C73451-A3001-B40
1.3	–	Front circuit board		-D31
1.4	(4) Figure 5-2	Screw SN 62217-B2,6×6-St-A3G	Order 5	H62217-B2506-Z1
1.5	(2) Figure 5-2	Seal		C73451-A3000-C31
1.6	(1) Figure 5-1	Set screw (M3)		D7964-L9010-S3
1.7	–	Rating plate cover		C73451-A3001 -C5
1.8		10 rating plate labels		-C16
1.9	–	Customer foil		-C44
2		**Enclosure**		
2.1	(6) Figure 5-3	Plastic housing		C73451-A3001-C3
2.2	(5) Figure 5-3	Blanking plates for unused slots		-A3000-C11
2.3	(1) Figure 5-3	PE conductor contact spring		-A3001-C8
2.4	–	Connection platen		-A3001-C25
2.5	–	Clamps	Order 2	-A3000-B20
3		**Power supply unit**		
3.1	(4) Figure 5-3	Power supply unit 24 V DC complete	without mains plug and fixing screws	C73451-A3001-B105
3.2	(4) Figure 5-3	Power supply unit 115/230 V AC complete		-B104
		Mains plug		
3.3	–	3–pin plug for 115/230 V AC IEC-320/V, DIN 49457A		C73334-Z343-C3
3.4		Special 2–pin plug for 24 V UC		C73334-Z343-C6
3.5	(2) Figure 5-3	Set screw (M4)		D7964-P8016-R
4		**Main board**		
4.1	(5) Figure 5-2	Main board*) complete		C73451-A3001-D32
4.2	–	14–pin plug		W73078-B1001-A714
4.3	–	10–pin plug		W73078-B1001-A710
5	–	**Options**	see chapter 6, page 175, Ordering Data	
5.1	–	4–pin terminal for 6DR2800-8I/8R/8P		W73078-B1001-A904
5.2	–	5–pin terminal for 6DR2801-8A/8B/8C and 6DR2802-8A		W73078-B1001-A705
5.3	–	6–pin terminal for 6DR2801-8D and 6DR2800-8A		W73078-B1001-A906
5.4	–	3–pin terminal for 6DR2804-8A/8B		W73078-B1001-A703
		6–pin terminal for 6DR2804-8A/8B		-A706
5.6	–	Jumpering plug for 6DR2800-8J/8R and main board C73451-A3001-D32		W73077-B2604-U2

*) (Basic card)

- **Ordering information**

The order must contain:

- Quantity
- Order number
- Description

For safety reasons, we recommend that you also specify the instrument type in your order.

- **Ordering example**

2 units	W73078-B1001-A714	
	14–pin plug	main circuit board DR24

6 Ordering Data

SIPART DR24, standard controller with

3 analog inputs 0/4 to 20 mA or 0/0.2 to 1 V or 0/2 to 10 V
3 analog outputs 0/4 to 20 mA
4 digital outputs 24 V
8 digital outputs 24 V

for power supply UC 24 V 6DR2410–4
for switchable power supply AC 115/230 V 6DR2410–5
Analog input module with 3AE for 0/4...20 mA or 0/0.2...1 V or 0/2...10 V 6DR2800-8A
Analog input module with 1AE for 0/4...20 mA or 0/0.2...1 V or 0/2...10 V 6DR2800-8J
Analog input module with 1 AE for resistance potentiometer 6DR2800–8R
UNI module 6DR2800-8V
Digital input module with 5 BE 24 V 6DR2801-8C
Digital output module with 2 BA relays (UC 35 V) 6DR2801-8D
Digital output module with 4 BA 24 V and 2 BE 6DR2801-8E
Analog output module with 1 AA (y_{HOLD}) 6DR2802-8A
Analog output module with 3 AA and 3 BE 6DR2802-8B
Interface relay module with 2 relays (AC 250 V) 6DR2804-8B
Interface relay module with 4 relays (AC 250 V) 6DR2804-8A
Interface module for V.28 point–to–point 6DR2803–8C
Interface module PROFIBUS DP . . . . . 6DR2803–8 P

Plug for the serial interface
9–pin D–plug for round cable (screw terminal) C73451-A347-D39
Bus plug connector for PROFIBUS DP . . . . . see catalog IK PI

User’s guide SIPART DR24 English C79000-G7476-C153
User’s guide SIPART DR24 German C79000-G7400-C153

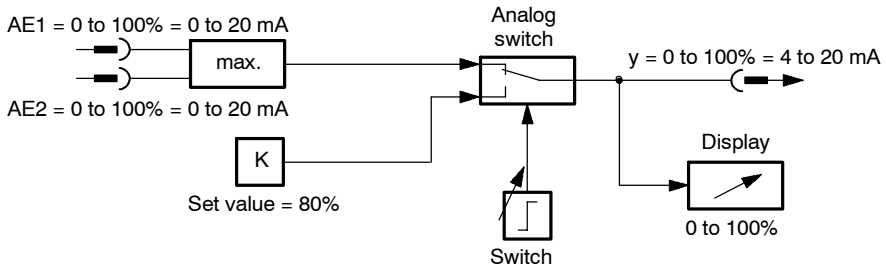
Operating Instructions ”Serial SIPART DR24 V.28 Bus Interface”
English C73000-B7476-C135
German C73000-B7400-C135

7 User Examples

7.1 Maximum Selection (Example 1)

- **Problem**

  Maximum selection with switchover possibility after set value K
  $y = \max (x_1, x_2) \text{ V } K$



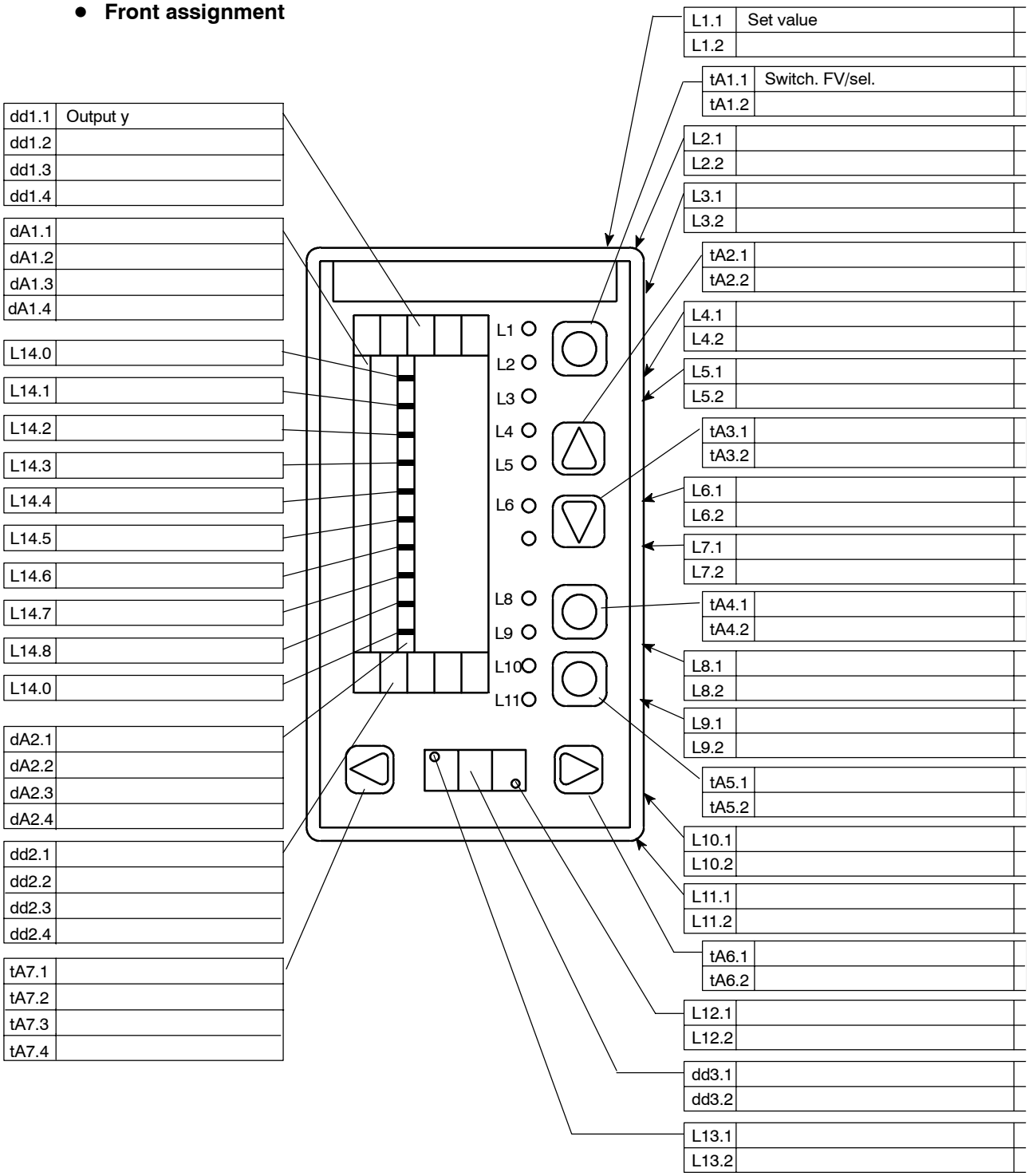
- **Interfaces of the SIPART DR24 to the process**

  2 analog inputs: AE1 = 0 to 20 mA; AE2 = 0 to 20 mA
  1 analog output AA: y = 4 to 20 mA

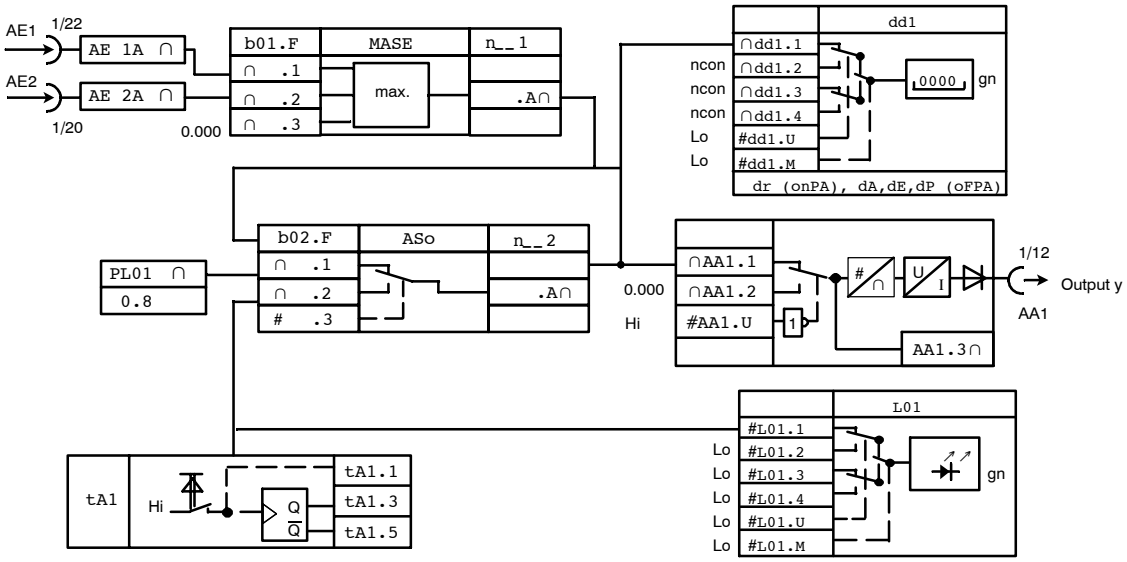
- **Equipment required**

  Standard SIPART DR24 controller

- **Front assignment**



- **Wiring diagram**



- **Parameterization and configuring lists** (other variables in factory setting)

hdEF

Question cycle dd2	Answer cycle dd1
AA1	4 MA
AE1	0 MA
AE2	0 MA
AEFr	50 H
nAME	1

FdEF

Question cycle dd2	Answer cycle dd1
b01.F	MASE
b02.F	ASo

FCon

Question cycle dd2	Answer cycle dd1
b01.1	AE1A
b01.2	AE2A
b01.3	0.000
b02.1	b01.A
b02.2	PL01
b02.3	tA1.3
AA1.1	b02.A
dd1.1	b02.A
L01.1	tA1.3

FPos

Question cycle dd2	Answer cycle dd1
n001	b01.F
n002	b02.F

oFPA

Question cycle		Answer cycle
dd2	dd3	dd1
dd1.1	dP	_ _ _ . -
	dA	0.0
	dE	100.0

Online parameter

Question cycle		Answer cycle
dd2	dd3	dd1
dd1.1	dr	1
PL01	-	0.800

7.2 Mathematical Link (Example 2)

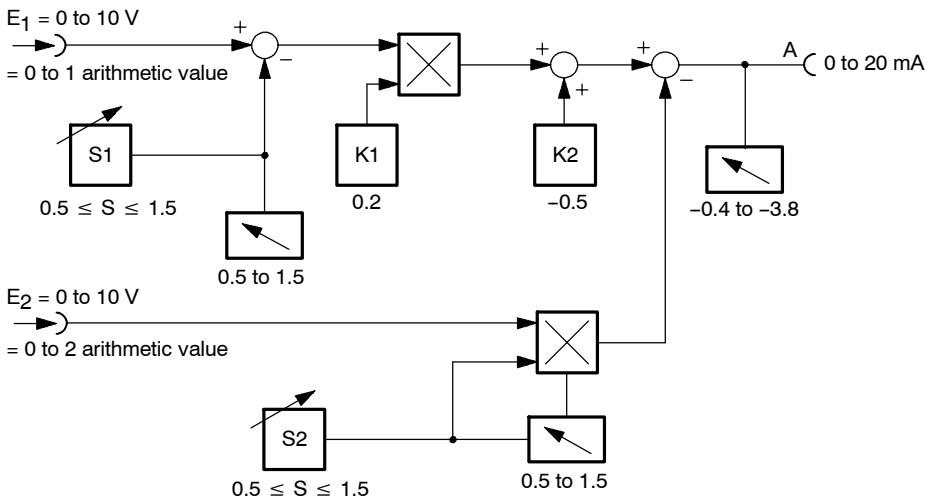
- **Problem**

  Output variable A as a function of two process variables E1 and E2:
  $A = K1 (E1 - S1) + K2 - S2 \cdot E2$

  E2 has double the value in relation to E1
  S1; S2 0.5 to 1.5 (variable parameters adjustable on the control and display unit)
  K1 0.2
  K2 −0.5 } set constants

  The result A is to be expressed as a calculated value across its entire range. The equation gives:

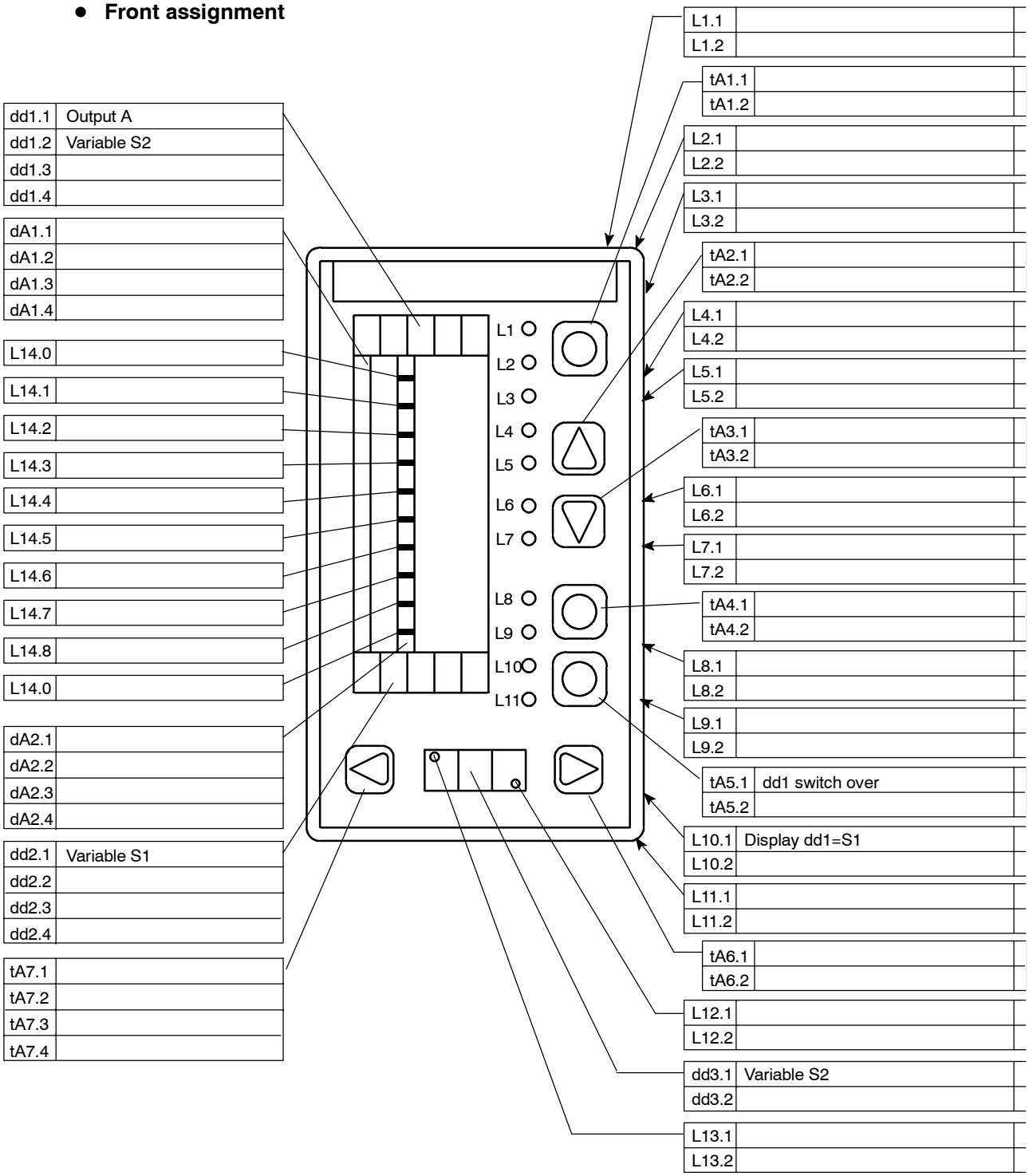
  $-3.8 \leq A \leq -0.4$



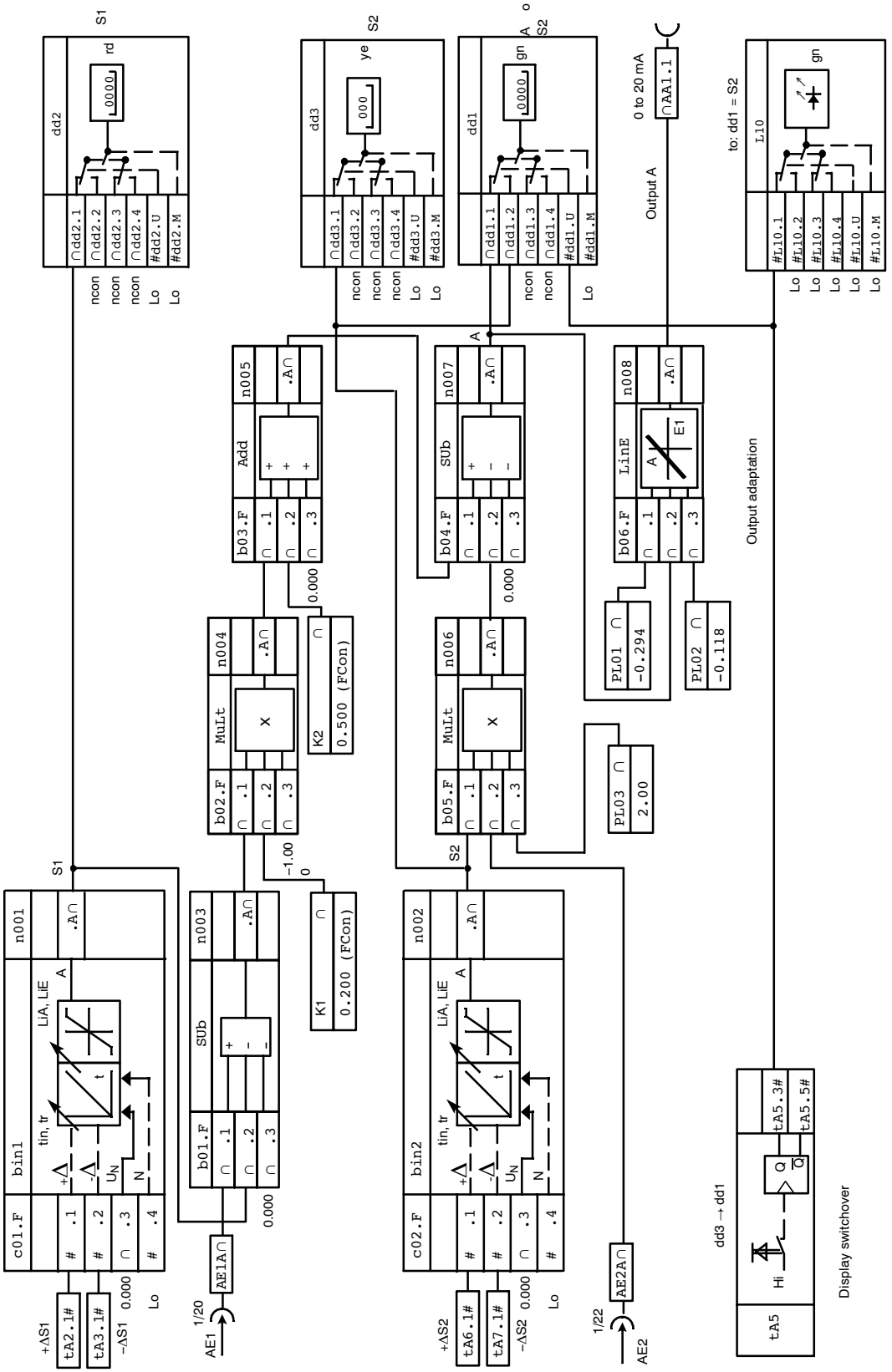
- **Interfaces of the multi−function unit to the process**
  2 analog inputs AE: E1 = 0 to 10 V; E2 = 0 to 10 V
  1 analog output AA: y = 0 to 20 mA ≙ A = −0.4 to −3.8 ≙ 0 to 100%

- **Equipment required**
  Standard SIPART DR24 controller

- **Front assignment**



- **Wiring diagram**



- **Parameterization and configuring lists** (other variables in factory setting)

hdEF

Question cycle dd2	Answer cycle dd1
AA1	0 MA
AE1	0 MA
AE2	0 MA
AEFr	50 H
nAME	2

FdEF

Question cycle dd2	Answer cycle dd1
b01.F	SUb
b02.F	MULt
b03.F	Add
b04.F	SUb
b05.F	MULt
b06.F	LinE
c01.F	bin1
c02.F	bin2

FCon

Question cycle dd2	Answer cycle dd1
b01.1	AE1A
b01.2	c01.A
b01.3	0.000
b02.1	b.01A
b02.2	0.200
b02.3	1.000
b03.1	b02.A
b03.2	-0.500
b03.3	0.000
b04.1	b03.A
b04.2	b05.a
b04.3	0.000
b05.1	c02.A
b05.2	AE2A
b05.3	PL03
b06.1	PL01
b06.2	b04.A
b06.3	PL02
c01.1	tA2.1
c01.2	tA3.1
c02.1	tA6.1
c02.2	tA7.1
AA1.1	b06.A
dd1.1	b04.A
dd1.2	c02.A
dd1.U	tA5.3
dd2.1	c01.A
dd3.1	c02.A
L10.1	tA5.3

FPos

Question cycle dd2	Answer cycle dd1
n001	c01.F
n002	c02.F
n003	b01.F
n004	b02.F
n005	b03.F
n006	b05.F
n007	b04.F
n008	b06.F

oFPA

Question cycle dd2	dd3	Answer cycle dd1
dd1.1	dP	_ _ . - -
	dA	0.00
	dE	1.00
dd1.2	dP	_ . - - -
	dA	0.000
	dE	1.000
dd2.1	dP	_ . - - -
	dA	0.000
	dE	1.000
dd3.1	dP	_ _ . -
	dA	0.0
	dE	1.0

Online parameter

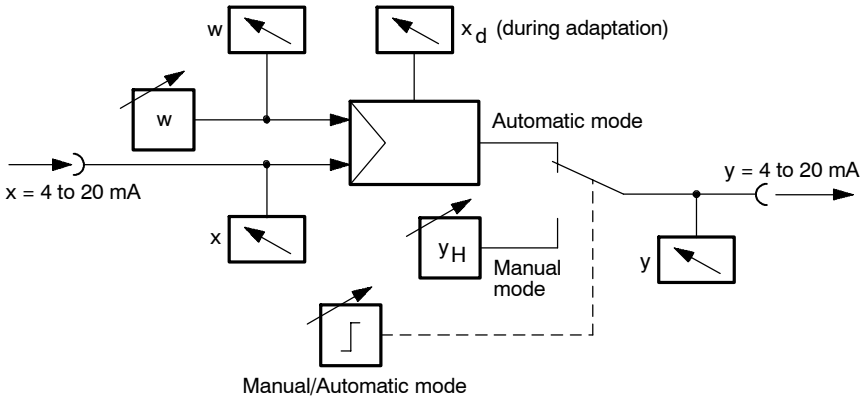
Question cycle dd2	dd3	Answer cycle dd1
dd1.1	dr	1
dd1.2	dr	1
dd2.1	dr	1
dd3.1	dr	1
PL01	-	-0.294
PL02	-	-0.118
PL03	–	2.000
bin 1	tin	ProG
	tr	oFF
	LiA	50.0
	LiE	150.0
bin 2	tin	ProG
	tr	oFF
	LiA	50.0
	LiE	150.0

7.3 Set Value Controller K (Example 3)

- **Problem: set value controller K with adaptation**

  Display switchover during adaptation w → xd

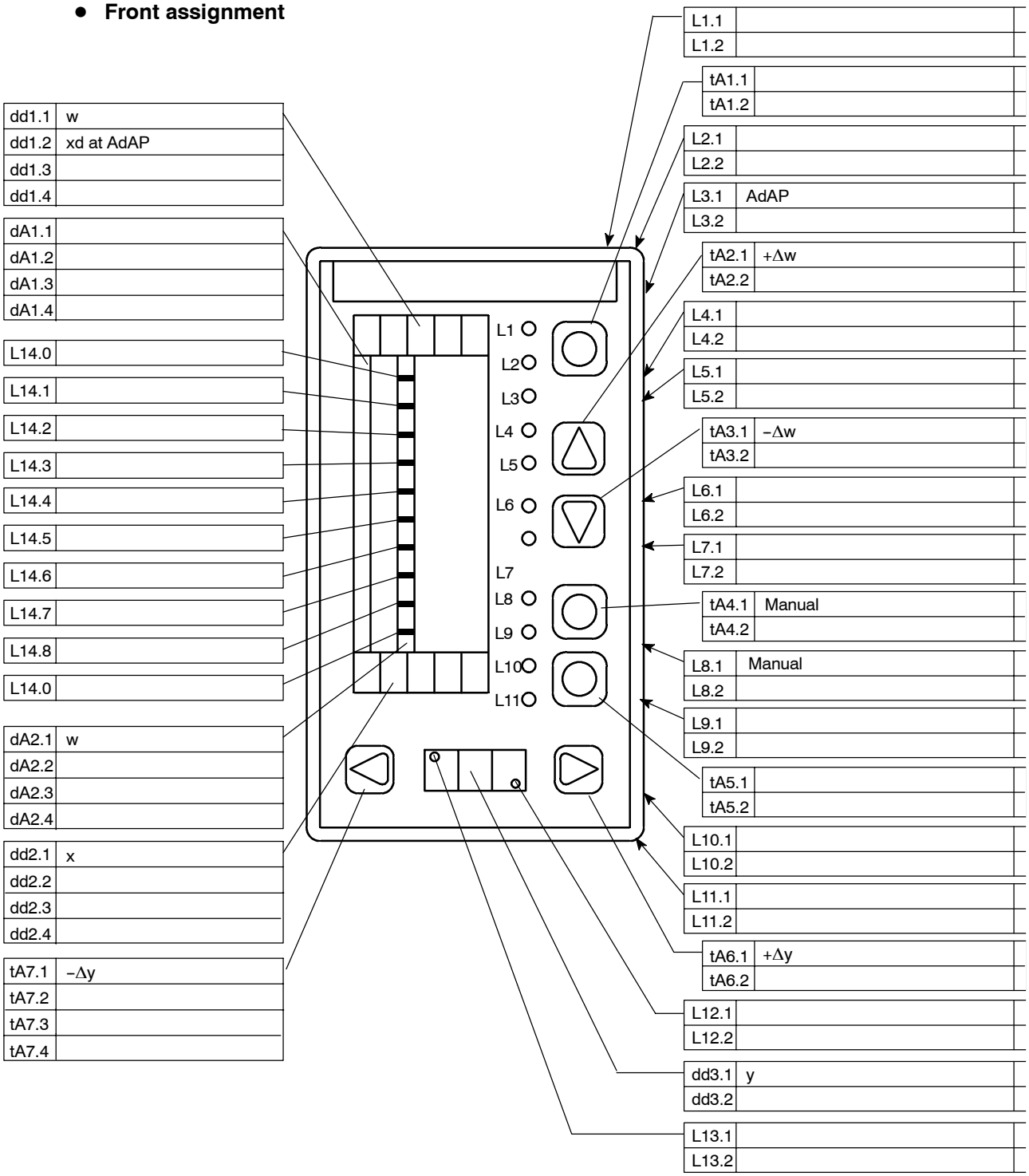
  The following should be displayed
  x, w 0 to 100 %
  y 0 to 100 %
  x_d –50 % to +50 %



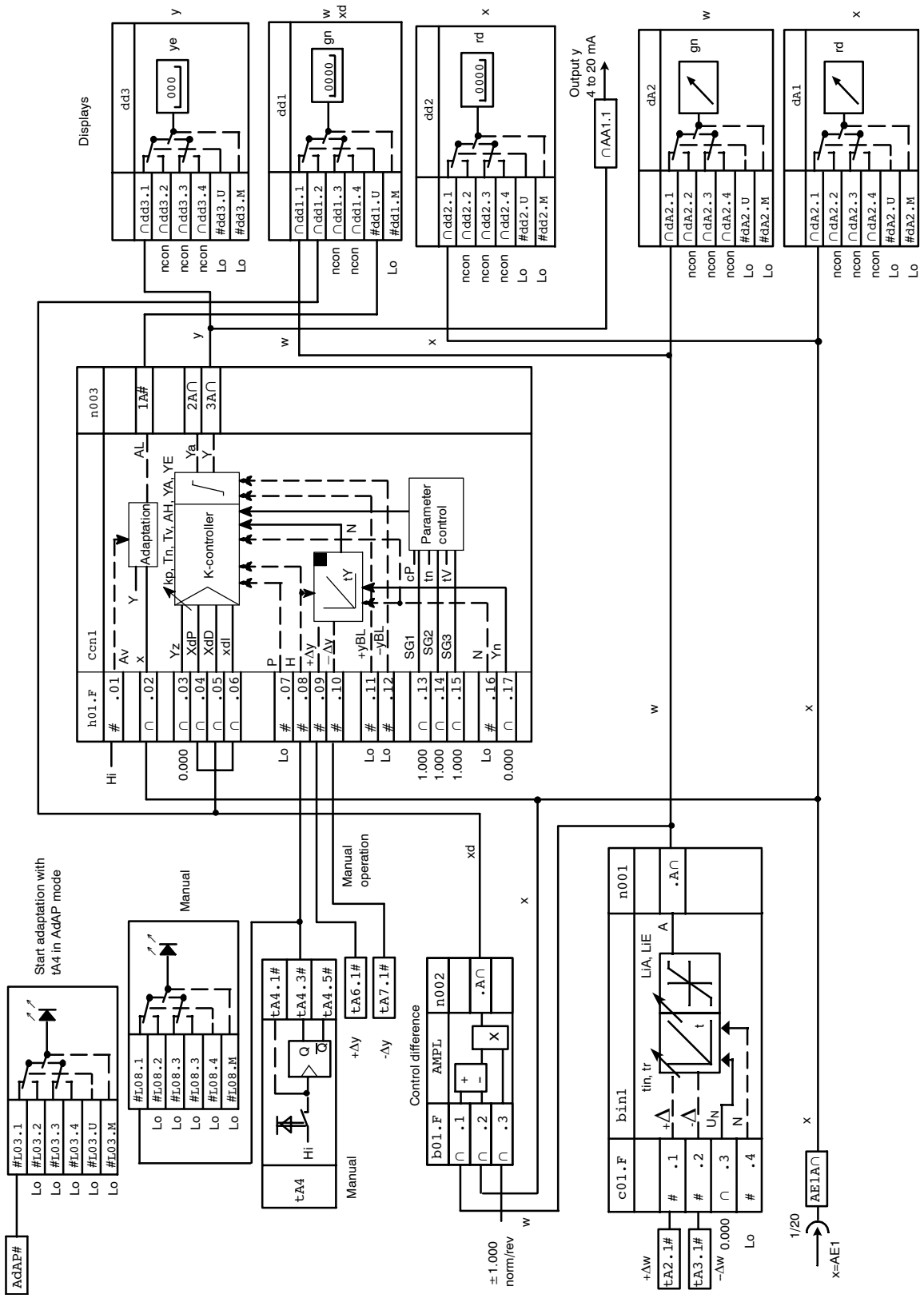
- **Interfaces of the multi–function unit to the process:**
  1 analog input AE: x= 4 to 20 mA
  1 analog output AA: y = 4 to 20 mA

- **Equipment required**
  Standard SIPART DR24 controller

- **Front assignment**



- **Wiring diagram**



- **Parameterization and configuring lists** (other variables in factory setting)

hdEF

Question cycle dd2	Answer cycle dd1
AA1	4 MA
AE1	4 MA
AEFr	50 H
nAME	3

FdEF

Question cycle dd2	Answer cycle dd1
b01.F	AMPL
c01.F	bin1
h01.F	Ccn1

FCon

Question cycle dd2	Answer cycle dd1
b01.1	c01.A
b01.2	AE1A
b01.3	1.000
c01.1	tA2.1
c01.2	tA3.1
c01.3	0.000
c01.4	Lo
h1.01	Hi
h1.02	AE1A
h1.03	0.000
h1.04	b01.A
h1.05	b01.A
h1.06	b01.A
h1.07	Lo
h1.08	tA4.3
h1.09	tA6.1
h1.10	tA7.1
h1.11	Lo
h1.12	Lo
h1.13	1.000
h1.14	1.000
h1.15	1.000
h1.16	Lo
h1.17	0.000
AA1.1	h1.3A
dA1.1	AE1A
dA1.2	ncon
dA1.U	Lo
dA2.1	c01.A
dA2.2	ncon
dA2.U	Lo
dd1.1	c01.A
dd1.2	b01.A
dd1.U	h1.1A
dd2.1	AE1A
dd2.2	ncon
dd2.U	Lo
dd3.1	h1.3A
dd3.2	ncon
dd3.U	Lo

FCon (continued)

Question cycle dd2	Answer cycle dd1
L03.1	AdAP
L03.2	Lo
L03.U	Lo
L08.1	tA4.3
L08.2	Lo
L08.U	Lo

FPos

Question cycle dd2	Answer cycle dd1
n001	c01.F
n002	b01.F
n003	h01.F

oFPA

Question cycle dd2	Question cycle dd3	Answer cycle dd1
dA1.1	dA	0.0
	dE	100.0
dA2.1	dA	0.0
	dE	100.0
dd1.1	dP	_ _ _ . -
	dA	0.0
	dE	100.0
dd1.2	dP	_ _ _ . -
	dA	0.0
	dE	100.0
dd2.1	dP	_ _ _ . -
	dA	0.0
	dE	100.0
dd3.1	dP	_ _ _
	dA	0
	dE	100

Online parameter

Question cycle dd2	Question cycle dd3	Answer cycle dd1
dd1.1	dr	1
dd1.2	dr	1
dd2.1	dr	1
dd3.1	dr	1
bin1	tin	ProG[1)]
	tr	oFF
	LiA	0.0
	LiE	100.0
Ccn1	CP	Definition at start up [1)]
	tn	
	tv	
	vv	
	AH	
	yo	
	Y_A	-5.0
	Y_E	105.0
	(ty)	60.00

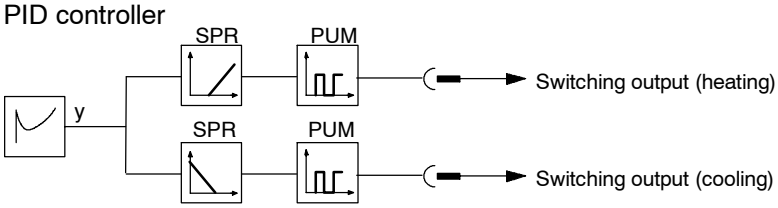
[1)] Start with factory setting, process–dependent

7.4 Two-position Controller for Heating and Cooling (Example 4)

- **Problem**

  Two function blocks ”split range” and two function blocks ”pulse width modulation” follow a continuous PID controller (see example 3) for the heating and cooling outputs.

PID controller

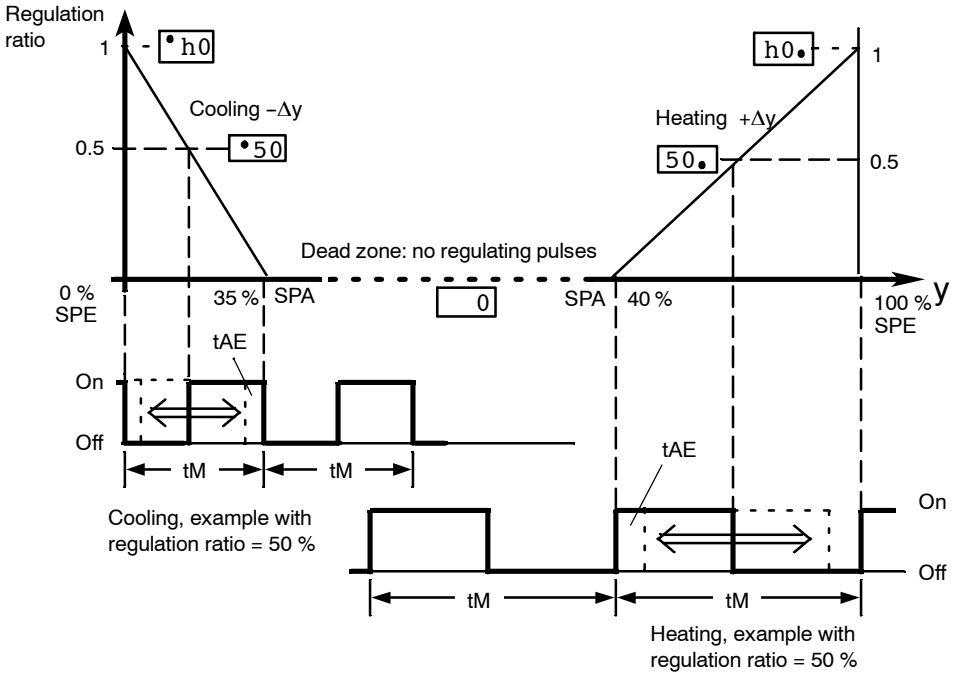


- **Interfaces of the multi–function unit to the process:**
  See example 3 additional 2 digital outputs BA

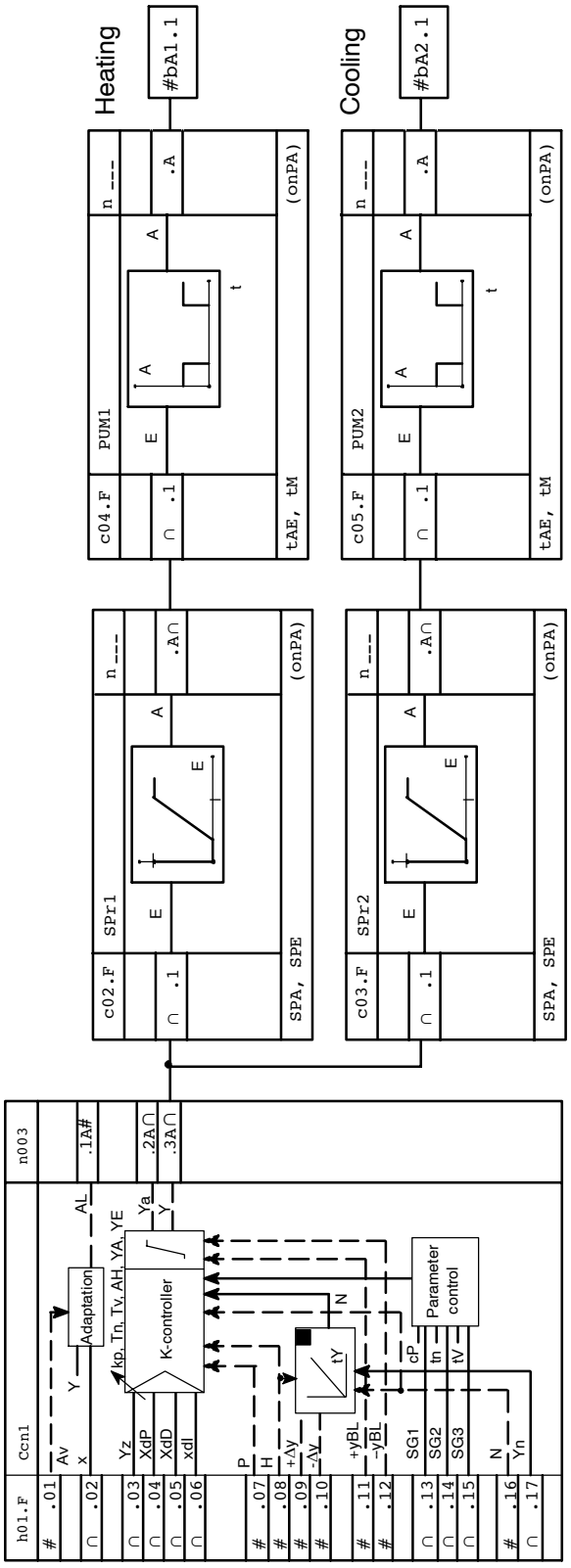
- **Equipment required**
  Standard SIPART DR24 controller
  Front assignment see example 3

Cooling:
Complex functions: SPr2 and PUM2
Section y = SPE (0 %) to SPA (cooling), −Δy
Period: tM from 0.1 to 1000 s
Minimum pulse length: tAE

Heating:
Complex functions: SPr1 and PUM1
Section y = SPA to SPE (100 %, heating), +Δy
Period: tM from 0.1 to 1000 s
Minimum pulse length: tAE



- **Wiring diagram** (example 4, supplement to the wiring diagram of example 3)



Two–position controller

The switching output can also supply continuous contact through y_a = -1 % and y_e = 101 % of the PID controller. The control loop is optimized with k_p, T_n, T_v.

The controller is adapted to the different line amplification of the heating and cooling channel with the parameters SPA, SPE.

The controller is adapted to the final control elements with the parameters tAE, tM.

See example 3 for complete K-controller.

• Parameterization and configuring lists

hdEF

Question cycle dd2	Answer cycle dd1
nAME	4

FdEF

Question cycle dd2	Answer cycle dd1
c02.F	SPr1
c03.F	SPr2
c04.F	PUM1
c05.F	PUM2

FCon

Question cycle dd2	Answer cycle dd1
c02.1	h1.3A
c03.1	h1.3A
c04.1	c02.A
c05.1	c03.A
bA1.1	c04.A
ba2.1	c05.A

FPos

Question cycle dd2	Answer cycle dd1
n002	c02.F
n003	c03.F
n004	c04.F
n005	c05.F

Online parameter

Question cycle dd2	Question cycle dd3	Answer cycle dd1
PUM1	tAE	20
PUM1	tM	1
PUM2	tAE	400
PUM2	tM	100
SPr1	SPA	40
SPr1	SPE	100
SPr2	SPA	35
SPr2	SPE	0

7.5 Switching Over the Display Levels (Process Operation Mode) (Example 5)

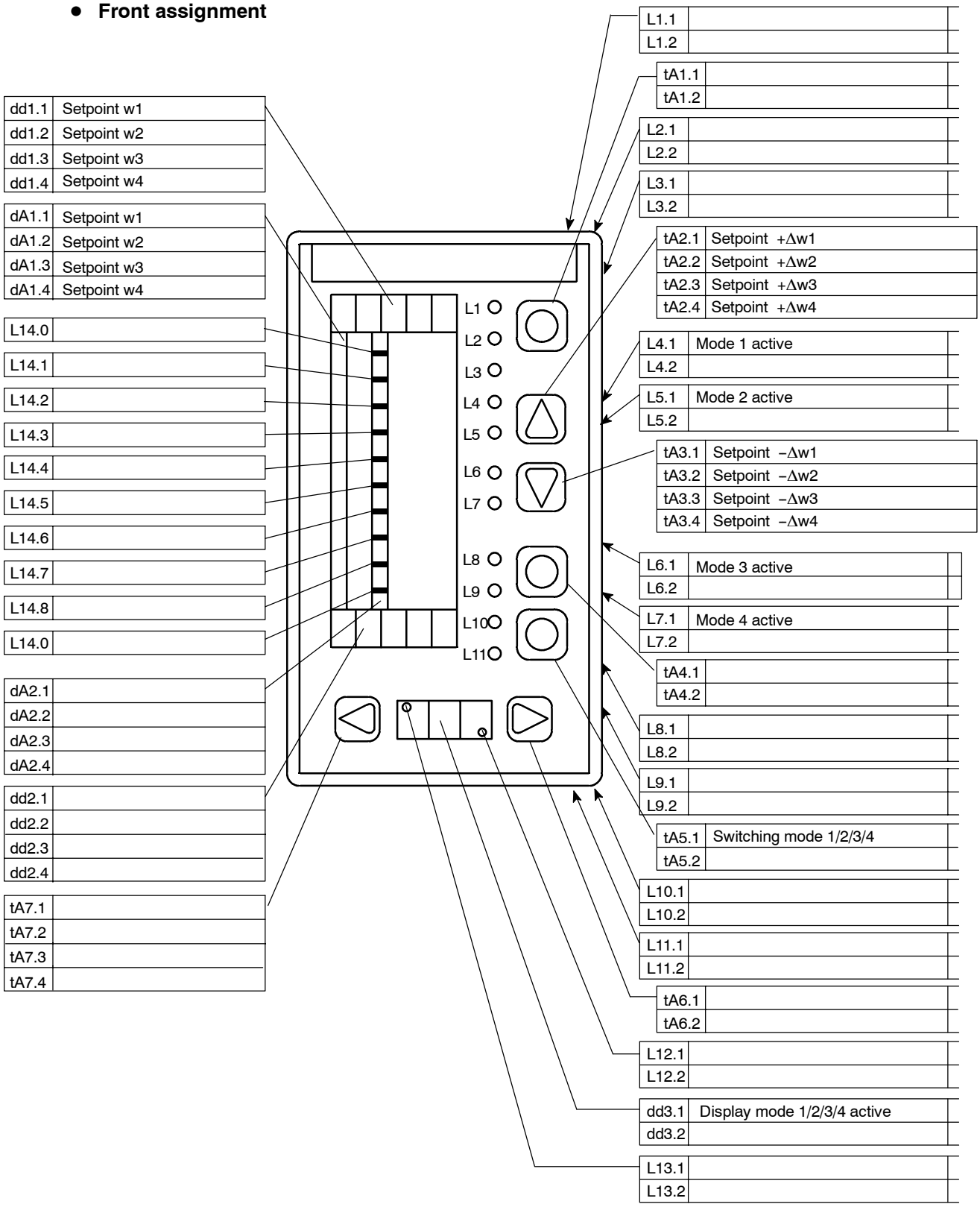
- **Problem**

  The operating panel should be switched in four modes with the key tA5. The ”active operating mode” is displayed by the diodes L4, L5, L6 and L7. At the same time the ”active operating mode” is shown on the display dd3.

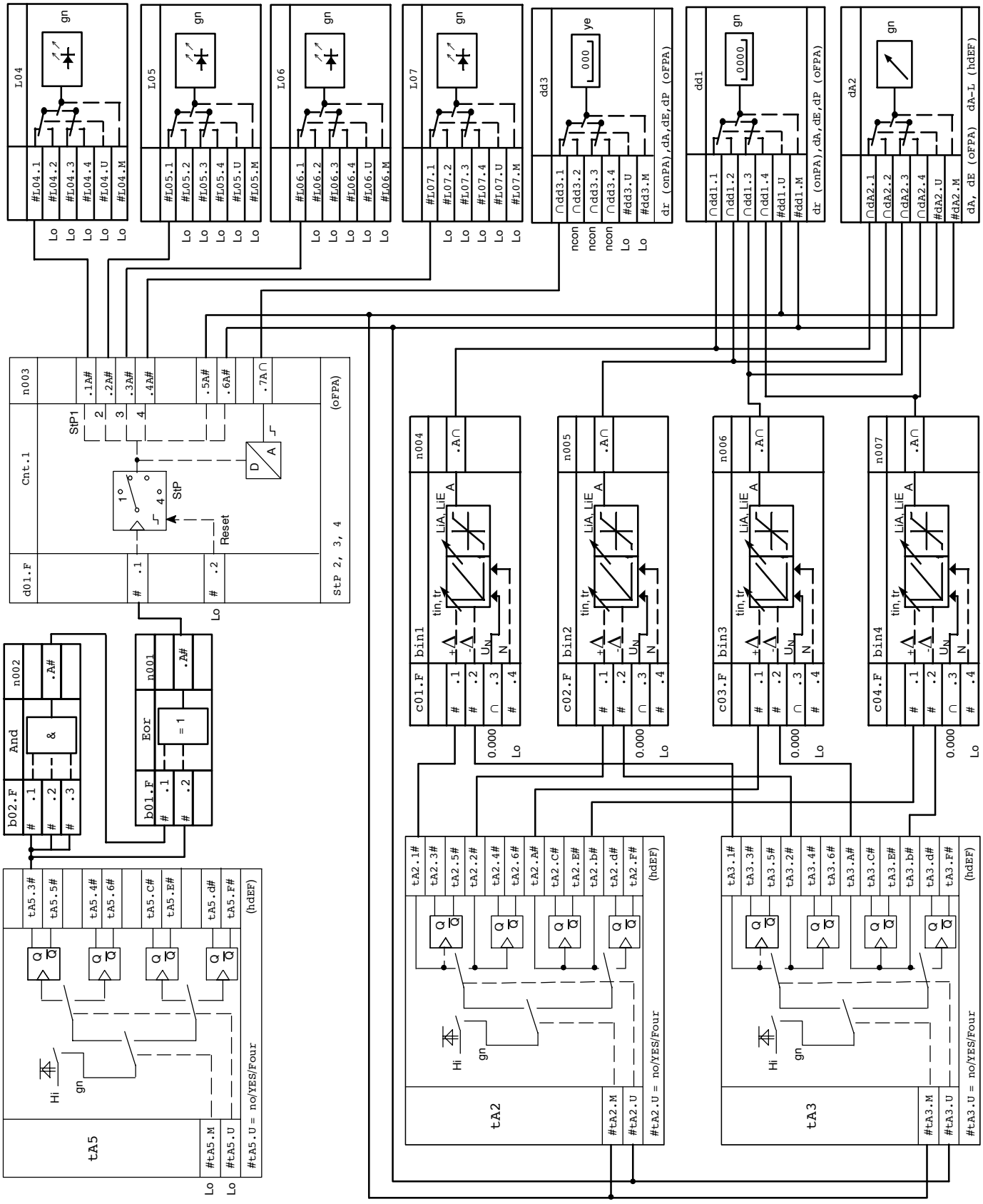
  The following control and display elements are to be switched
  Displays: dA1, dd1
  Keys: tA2, tA3

  Four internal setpoints are set by the keys tA2, tA3 which are displayed on dA1, dd1.

- **Front assignment**



- **Wiring diagram**



- **Parameterization and configuring lists** (other variables in factory setting)

  This example can be used as a basis for assembling a multiple controller in connection with user example 3.

hdEF

Question cycle dd2	Answer cycle dd1
nAME	4
tA2.U	Four
tA3.U	Four

FdEF

Question cycle dd2	Answer cycle dd1
b01.F	Eor
b02.F	And
c01.F	bin1
c02.F	bin2
c03.F	bin3
c04.F	bin4
d01.F	Cnt1

FCon

Question cycle dd2	Answer cycle dd1
b01.1	b02.A
b01.2	tA5.3
b02.1	tA5.3
b02.2	tA5.3
b02.3	tA5.3
c01.1	tA2.1
c01.2	tA3.1
c02.1	tA2.2
c02.2	tA3.2
c03.1	tA2.A
c03.2	tA3.A
c04.1	tA2.b
c04.2	tA3.b
d1.01	b01.A
L04.1	d1.1A
L05.1	d1.2A
L06.1	d1.3A
L07.1	d1.4A
dA2.1	c01.A
dA2.2	c02.A
dA2.3	c03.A
dA2.4	c04.A
dA2.M	d1.6A
dA2.U	d1.5A
dd1.1	c01.A
dd1.2	c02.A
dd1.3	c03.A
dd1.4	c04.A
dd1.M	d1.6A
dd1.U	d1.5A
dd3.1	d1.7A

FCon

Question cycle dd2	Answer cycle dd1
tA2.M	d1.6A
tA2.U	d1.5A
tA3.M	d1.6A
tA3.U	d1.5A

FPos

Question cycle dd2	Answer cycle dd1	
n001	b01.F	*)
n002	b02.F	*)
n003	d01.F	
n004	c01.F	
n005	c02.F	
n006	c03.F	
n007	c04.F	

Offline parameters

Question cycle dd2	Question cycle dd3	Answer cycle **dd1**
dA2.1	dA	0.0
dA2.1	dE	100
dA2.2	dA	0.0
dA2.2	dE	100
dA2.3	dA	0.0
dA2.3	dE	100
dA2.4	dA	0.0
dA2.4	dE	100
dd1.1	dP	_ _ _ . -
dd1.1	dA	0.0
dd1.1	dE	100.0
dd1.2	dP	_ _ _ . -
dd1.2	dA	0.0
dd1.2	dE	100.0
dd1.3	dP	_ _ _ . -
dd1.3	dA	0.0
dd1.3	dE	100.0
dd1.4	dP	_ _ _ . -
dd1.4	dA	0.0
dd1.4	dE	100.0
dd3.1	dP	_ _ _
dd3.1	dA	0
dd3.1	dE	100
Cnt1	StP	4

Note: The order b01.F before b02.F (processing Eor before And) is not absolutely necessary for this function.

8 Programming Aids

Guidelines for creating an application program for the SIPART D24 controller

- **Define task clearly**

  - Plant mimic, block diagram
  - Mathematical perspectives/equations
  - Special conditions, e.g. limit values, use of safety values, signal operating modes, start–stop criteria, interlocks, reaction when reaching or exceeding limit values, restart conditions etc.

- **Clarify and define interfaces of the SIPART DR24 to the process**

  - Number and type of input and output variables (analog, digital, SES)
  - Measuring ranges, signal ranges, significance
  - Variables to be displayed
  - Manual intervention possibilities with front keys, adjust variables, select variables/sequences

- **SIPART DR24, version, connections**

  - Define version/equipment with signal convertors
    Note accessories such as relay module, SES component
  - Define interface assignments
  - Define position of the jumpers on the main board and signal convertors,
    e.g. 0/4–20 mA
  - Determine the external load of the SIPART DR24 by BA and L+ supplied instruments, if greater than allowed, provide external power supply or supply additional instruments from remote source.

- **Define front panel assignment**

  - Display dA2 as analog display or L14.0 to 14.9
  - Displays: variables, measuring ranges, signal ranges, display ranges, Hi/Lo significance
  - Switched variable, pushbutton: assigned LED: Hi/Lo significance
  - Define labeling for rating plate and label on front panel

- **Draw wiring diagram of the SIPART DR24**

  - Design block diagram of the function process, relationships of input range, function range, output range; define links e.g. for bumpless switchover, tracking, blocking, external feedback if necessary.
    Define parameters (number and value)
  - Transform block diagram to basic function blocks of arithmetic block numbers and basic functions. Connect basic and complex function blocks with each other and with the input and output functions. Connect the data sinks to the corresponding data sources
  - Position function blocks
    Define the processing sequence so that the individual arithmetic operations are performed sequentially using up-to-date data.

- **Table**

  - Define programs
  - Write configuring lists for hdEF, FdEF, FCon FPoS, oFPA, CLPA, CAE4/5
  - Write parameterization lists (onPA)

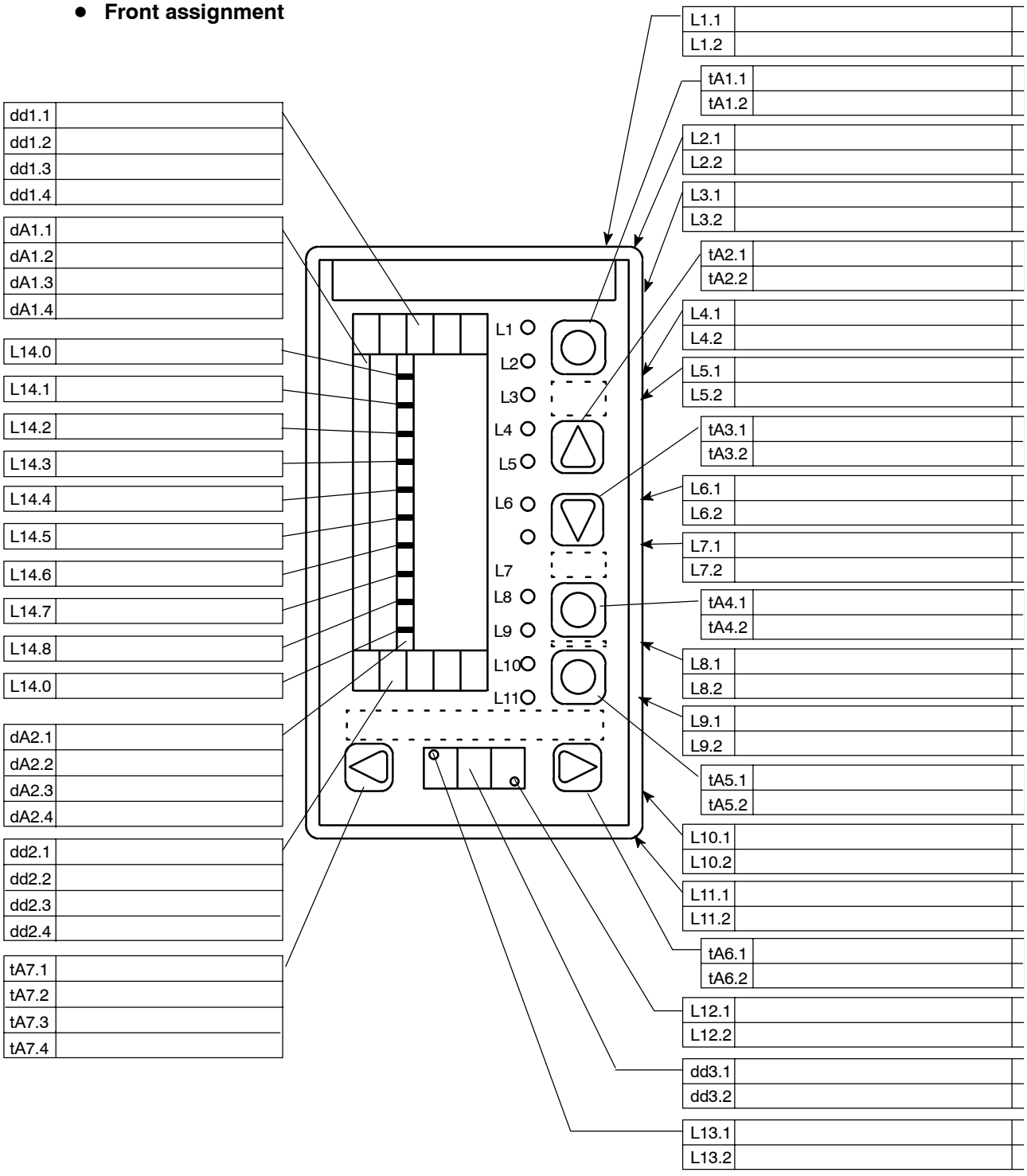
- **SIPART DR24 Configuring and Parameterization**

  - Set jumpers on main board and signal convertors.
  - Reset user program memory to factory setting (APSt)
  - Configuring and parameterization
  - Check configured and parameterized functions against specification

- **Collate and correct program documentation**

  - Programs, users' measuring point numbers
  - Task definition
  - SIPART DR24 version, order number, option modules
  - Connection diagram
  - Front assignment and labeling
  - Wiring diagram
  - Configuring lists
  - Parameterization lists including the usual operational parameters, e.g. control parameters.

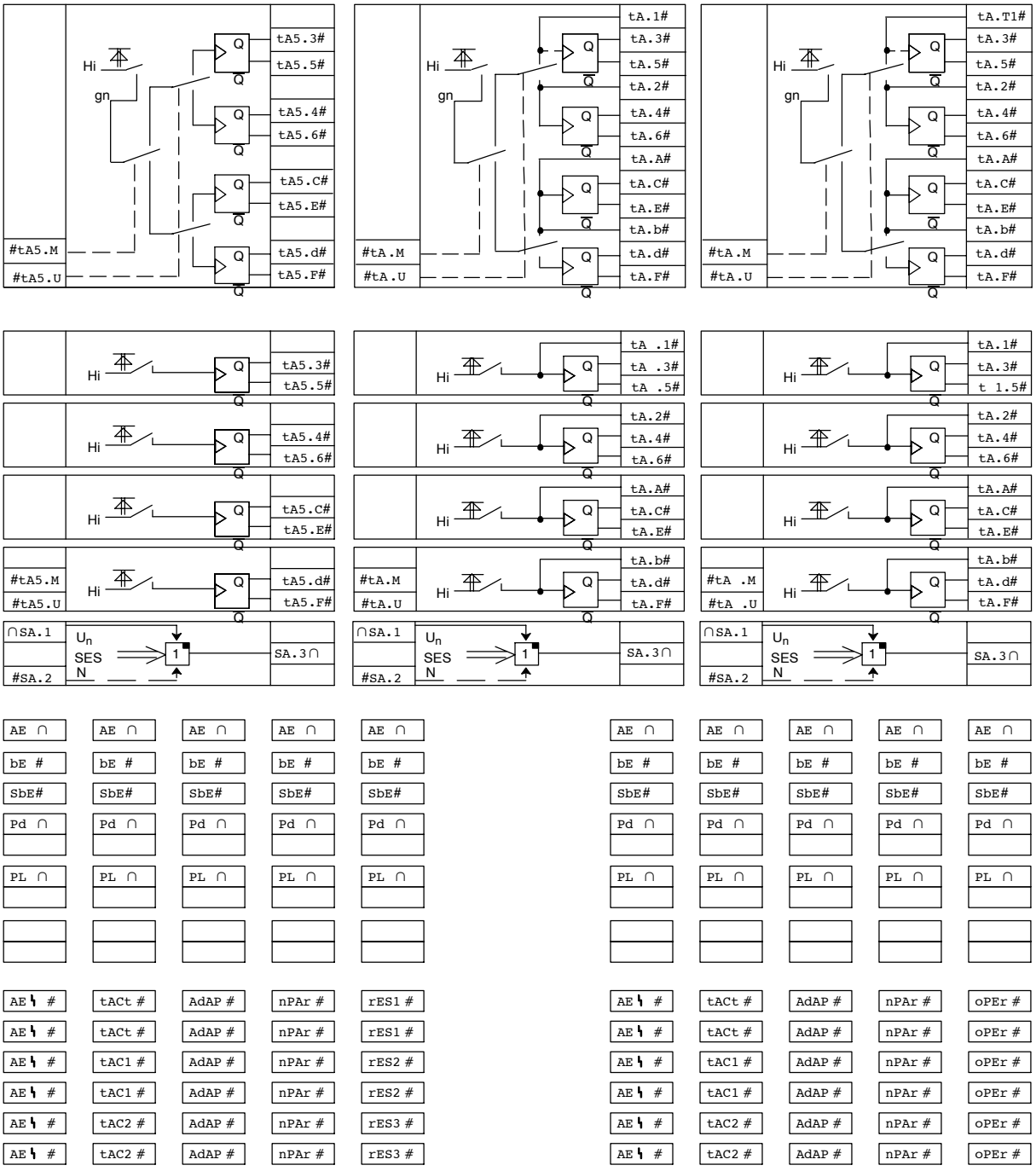
- **Front assignment**



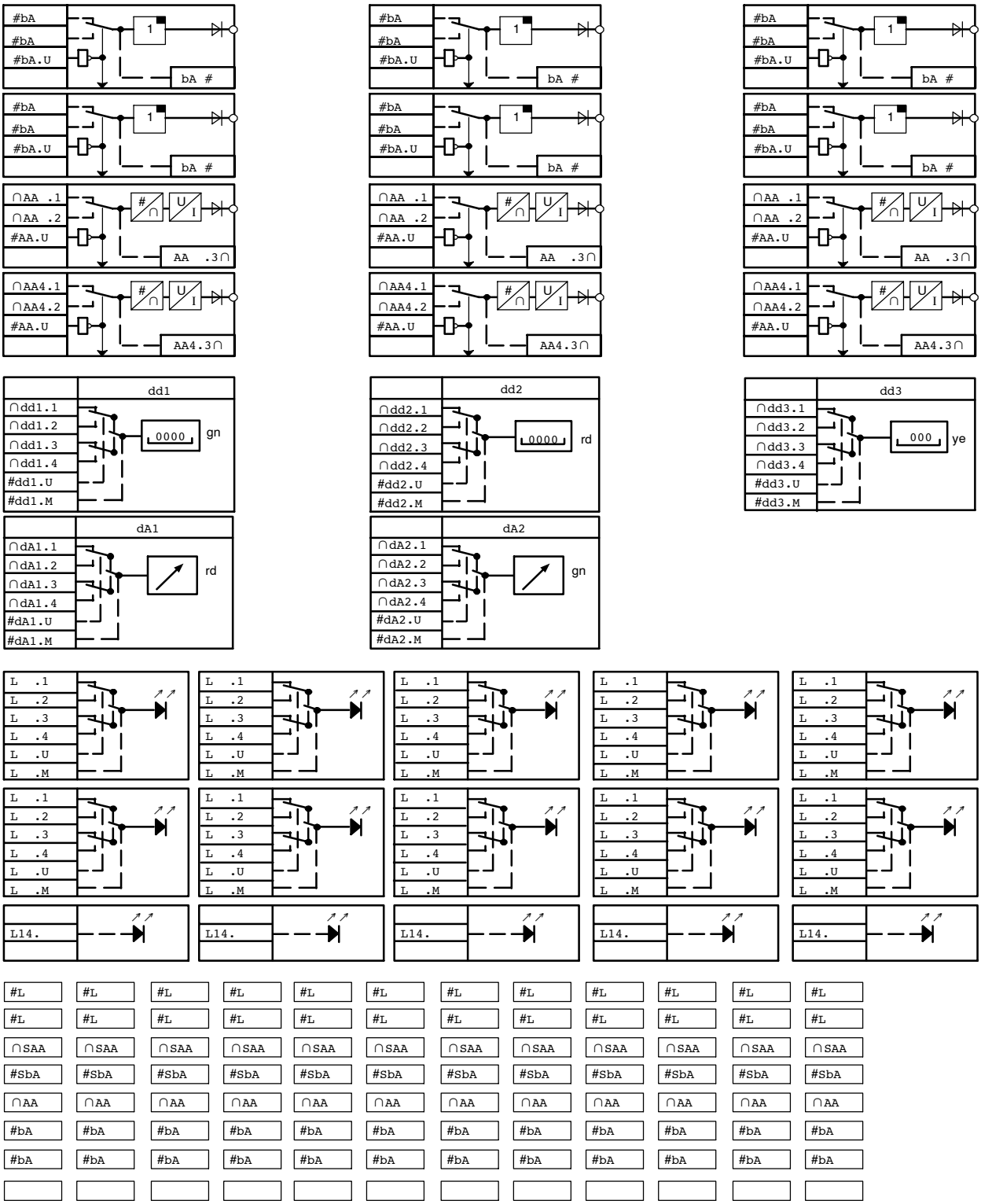
- **Front assignment** (continued)

L1.3	
L1.4	
tA1.3	
tA1.4	
L2.3	
L2.4	
L3.3	
L3.4	
tA2.3	
tA2.4	
L4.3	
L4.4	
L5.3	
L5.4	
tA3.3	
tA3.4	
L6.3	
L6.4	
L7.3	
L7.4	
tA4.3	
tA4.4	
L8.3	
L8.4	
L9.3	
L9.4	
tA5.3	
tA5.4	
L10.3	
L10.4	
L11.3	
L11.4	
tA6.3	
tA5.4	
L12.3	
L12.4	
dd3.3	
dd3.4	
L13.3	
L13.4	

- **Connection plan templates input functions**



- **Connection plan templates output range**



- **Connection plan templates arithmetic blocks**

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b_.E		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

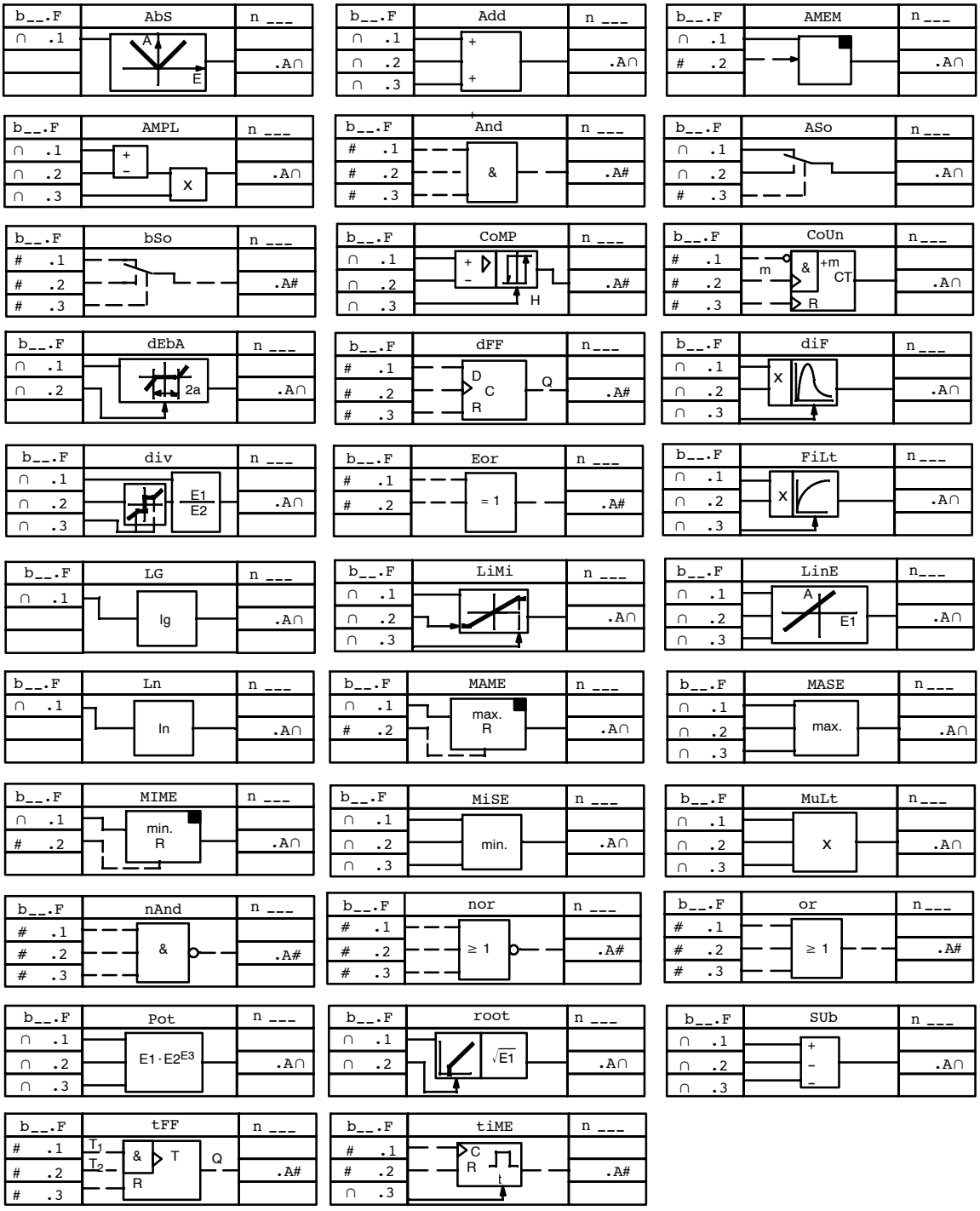
b__.F		n ___
.1		
.2		.A
.3		

b__.F		n ___
.1		
.2		.A
.3		

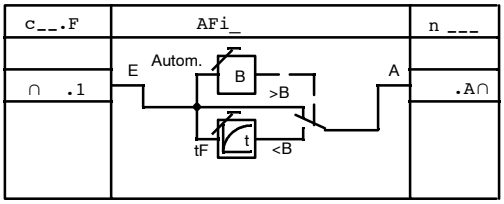
b__.F		n ___
.1		
.2		.A
.3		

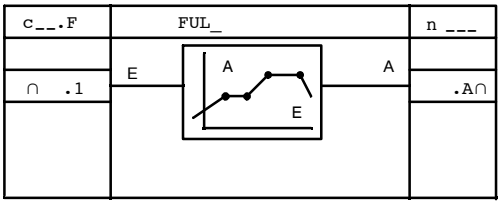
b__.F		n ___
.1		
.2		.A
.3		

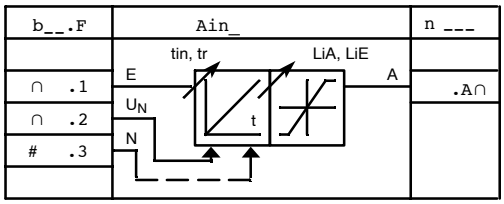
- **Basic functions of the SIPART DR24**

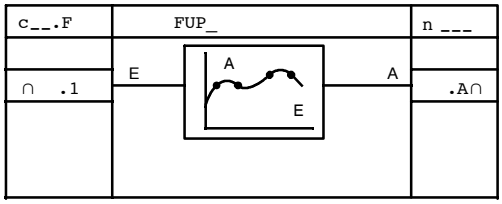


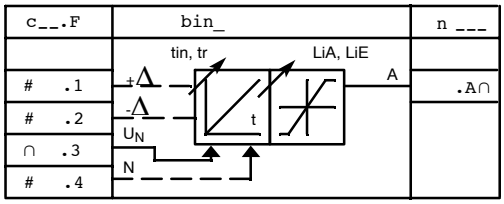
- **Complex functions c and d of the SIPART DR24**

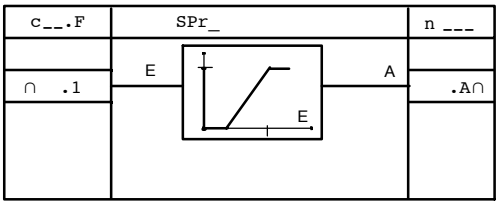


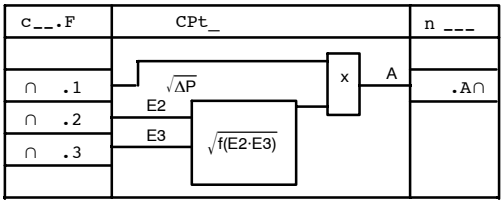


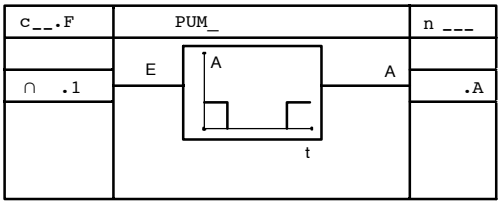


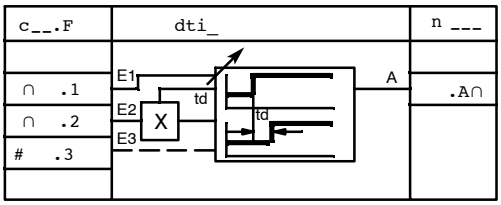


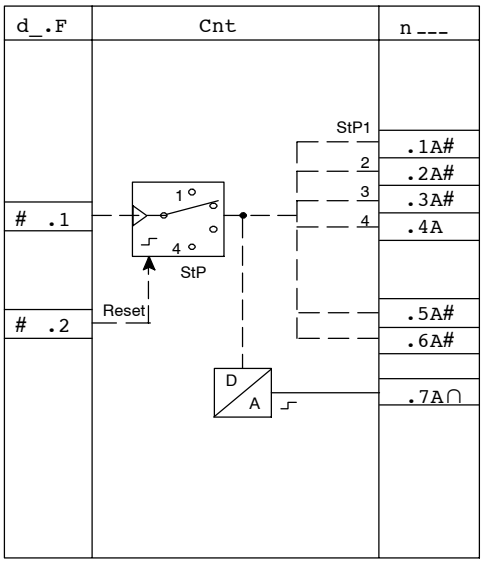


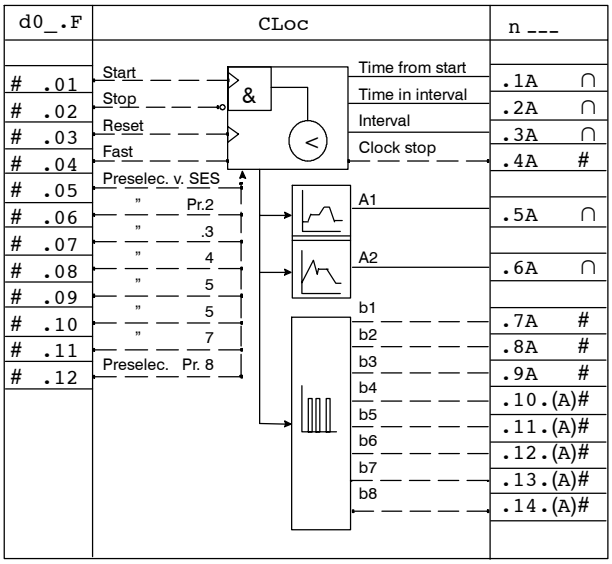


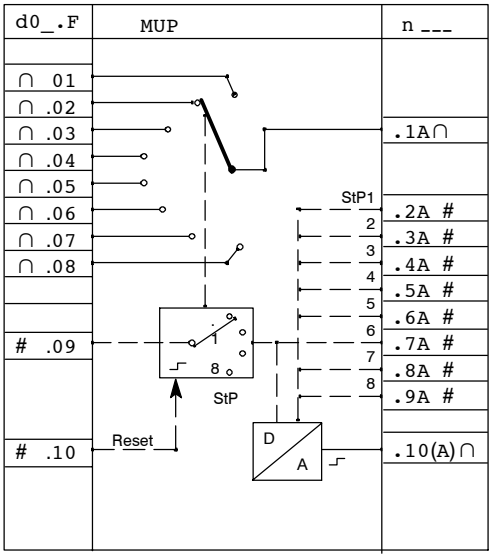




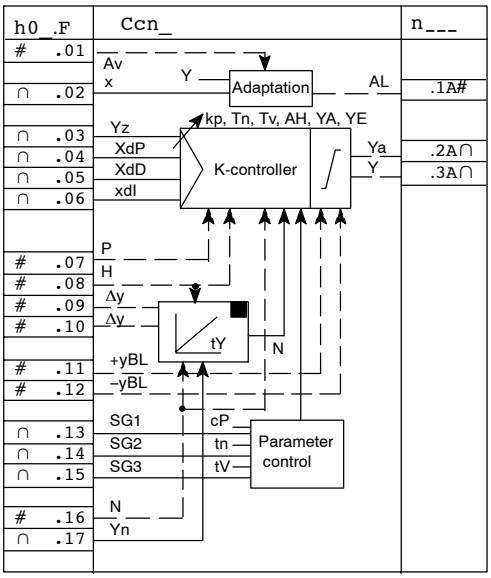


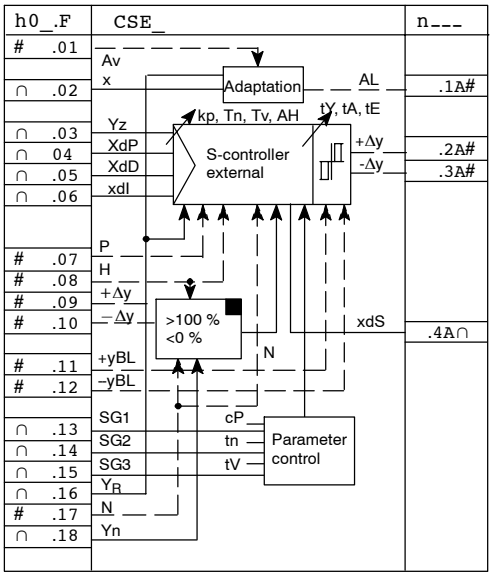

d_.F
Cnt
n ___
StP1
.1A#
2
.2A#
3
.3A#
.1
4
.4A
1
4
StP
Reset
.2
.5A#
.6A#
D
A
.7A∩

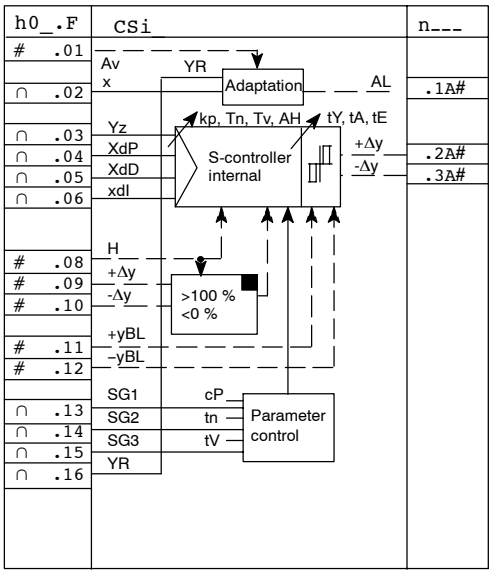

d0_.F
CLoc
n ___
Start
Stop
Reset
Fast
Preselec. v. SES
" Pr.2
" .3
" 4
" 5
" 5
" 7
Preselec. Pr. 8
.01
.02
.03
.04
.05
.06
.07
.08
.09
.10
.11
.12
&
<
Time from start
Time in interval
Interval
Clock stop
A1
A2
b1
b2
b3
b4
b5
b6
b7
b8
.1A ∩
.2A ∩
.3A ∩
.4A #
.5A ∩
.6A ∩
.7A #
.8A #
.9A #
.10.(A)#
.11.(A)#
.12.(A)#
.13.(A)#
.14.(A)#


d0_.F
MUP
n ___
∩ 01
∩ .02
∩ .03
∩ .04
∩ .05
∩ .06
∩ .07
∩ .08
.09
.10
.1A∩
StP1
.2A #
2
.3A #
3
.4A #
4
.5A #
5
.6A #
6
.7A #
7
.8A #
8
.9A #
1
8
StP
Reset
D
A
.10(A)∩

- **Complex functions h (controller) of the SIPART DR24**







Configuring list FdEF

Program name:	Processor:	Date:
Customer/system:		Page:

Basic functions

Question dd2	Answer dd1	Question dd2	Answer dd1	Question dd2	Answer dd1	Answer cycle dd1
Arithmetic block	Basic function	Arithmetic block	Basic function	Arithmetic block	Basic function	
b01.F		b34.F		b67.F		ndEF
b02.F		b35.F		b68.F		AbS
b03.F		b36.F		b69.F		Add
b04.F		b37.F		b70.F		AMEM
b05.F		b38.F		b71.F		AMPL
b06.F		b39.F		b72.F		And
b07.F		b40.F		b73.F		ASo
b08.F		b41.F		b74.F		bSO
b09.F		b42.F		b75.F		CoMP
b10.F		b43.F		b76.F		CoUn
b11.F		b44.F		b77.F		dEbA
b12.F		b45.F		b78.F		dFF
b13.F		b46.F		b79.F		diF
b14.F		b47.F		b80.F		div
b15.F		b48.F		b81.F		Eor
b16.F		b49.F		b82.F		FiLt
b17.F		b50.F		b83.F		LG
b18.F		b51.F		b84.F		LiMi
b19.F		b52.F		b85.F		LinE
b20.F		b53.F		b86.F		LN
b21.F		b54.F		b87.F		MAME
b22.F		b55.F		b88.F		MASE
b23.F		b56.F		b89.F		MiME
b24.F		b57.F		b90.F		MiSE
b25.F		b58.F		b91.F		MULt
b26.F		b59.F		b92.F		nAnd
b27.F		b60.F		b93.F		nor
b28.F		b61.F		b94.F		or
b29.F		b62.F		b95.F		Pot
b30.F		b63.F		b96.F		root
b31.F		b64.F		b97.F		Sub
b32.F		b65.F		b98.F		tFF
b33.F		b66.F		b99.F		tiME

Configuring list FdEF

Program name:	Processor:	Date:
Customer/system:		Page:

Basic functions

Question dd2	Answer dd1	Question dd2	Answer dd1	Question dd2	Answer dd1	Answer cycle dd1
Arithmetic block	Basic function	Arithmetic block	Basic function	Arithmetic block	Basic function	
bh0.F						ndEF
bh1.F						AbS
bh2.F						Add
bh3.F						AMEM
bh4.F						AMPL
bh5.F						And
bh6.F						ASo
bh7.F						bSO
bh8.F						CoMP
bh9.F						CoUn
						dEbA
						dFF
						diF
						div
						Eor
						FiLt
						LG
						LiMi
						LinE
						LN
						MAME
						MASE
						MiME
						MiSE
						MULt
						nAnd
						nor
						or
						Pot
						root
						Sub
						tFF
						tiME

Configuring list FdEF

Program name:	Processor:	Date:
Customer/system:		Page:

FdEF, Complex functions

Question dd2	Answer dd1	Answer cycle dd1	Question dd2	Answer dd1	Answer cycle dd1
Arithmetic block	Complex function		Arithmetic block	Complex function	
c01.F		ndEF	d01.F		ndEF
c02.F		AFi1	d02.F		CLoc
c03.F		AFi2	d03.F		Cnt1
c04.F		Ani1	d04.F		MUP1
c05.F		Ani2			MUP2
c06.F		Ani3			
c07.F		Ani4			
c08.F		bin1	h01.F		ndEF
c09.F		bin2	h02.F		Ccn1
c10.F		bin3	h03.F		Ccn2
c11.F		bin4	h04.F		Ccn3
c12.F		bin5			Ccn4
c13.F		bin6			CSE1
c14.F		CPt1			CSE2
c15.F		CPt2			CSE3
c16.F		dti1			CSE4
C17.F		dti2			CSi1
c18.F		FUL1			CSi2
C19.F		FUL2			CSi3
C20.F		FUP1			CSi4
C21.F		FUP2			
C22.F		PUM1			
C23.F		PUM2			
C24.F		PUM3			
C25.F		PUM4			
C26.F		SPr1			
C27.F		SPr2			
C28.F		SPr3			
C29.F		SPr4			
C30.F		SPr5			
C31.F		SPr6			
C32.F		SPr7			
C33.F		Spr8			

Configuring list hdEF

Program name:	Processor:	Date:
Customer/system:		Page:

hdEF

Question dd2	Answer dd1	Answer cycle dd1	Question dd2	Answer dd1	Answer cycle dd1
AA1			dA–L		dA2, L14
AA2			dPon		no, YES
AA3			nAME		0 to 254
AA4			OP5		no, 4bA, 5bE, 2rEL, 1AA, 3AE, 3AA
AA5		0MA, 4MA			
AA6			OP6		no, 4bA, 5bE, 2rEL, 1AA, 3AE, 3AA
AA7					
AA8					
AA9			SES		no, YES
AAU		no, YES	tA1.U		no, YES, Four
AE1		no, 0MA, 4MA	tA2.U		
AE2			tA3.U		
AE3			tA4.U		
AE4		no, 0MA, 4MA Uni_, Uni¯	tA5.U		
AE5			tA6.U		
AE6		0MA, 4MA	tA7U		
AE7					
AE8					
AE9					
AE10					
AE11					
AEFr		50Hz, 60Hz, YES, no			
bAtt					
bAU					

[1] Position 0 cannot be set manually.

Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data sink	Answer dd1 Data source	Question dd2 Data sinks	Answer dd1 Data source	Question dd2 Data sinks	Answer dd1 Data source
b01.1		b14.1		b27.1	
b01.2		b14.2		b27.2	
b01.3		b14.3		b27.3	
b02.1		b15.1		b28.1	
b02.2		b15.2		b28.2	
b02.3		b15.3		b28.3	
b03.1		b16.1		b29.1	
b03.2		b16.2		b29.2	
b03.3		b16.3		b29.3	
b04.1		b17.1		b30.1	
b04.2		b17.2		b30.2	
b04.3		b17.3		b30.3	
b05.1		b18.1		b31.1	
b05.2		b18.2		b31.2	
b05.3		b18.3		b31.3	
b06.1		b19.1		b32.1	
b06.2		b19.2		b32.2	
b06.3		b19.3		b32.3	
b07.1		b20.1		b33.1	
b07.2		b20.2		b33.2	
b07.3		b20.3		b33.3	
b08.1		b21.1		b34.1	
b08.2		b21.1		b34.2	
b08.3		b21.3		b34.3	
b09.1		b22.1		b35.1	
b09.2		b22.2		b35.2	
b09.3		b22.3		b35.3	
b10.1		b23.1		b36.1	
b10.2		b23.2		b36.2	
b10.3		b23.3		b36.3	
b11.1		b24.1		b37.1	
b11.2		b24.2		b32.2	
b11.3		b24.3		b37.3	
b12.1		b25.1		b38.1	
b12.2		b25.2		b38.2	
b12.3		b25.3		b38.3	
b13.1		b26.1		b39.1	
b13.2		b26.2		b39.2	
b13.3		b26.3		b39.3	

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ᒐ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ᒐ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEᒐ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

1) has the meaning dark for display

Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
b40.1		b53.1		b66.1	
b40.2		b53.2		b66.2	
b40.3		b53.3		b66.3	
b41.1		b54.1		b67.1	
b41.2		b54.2		b67.2	
b41.3		b54.3		b67.3	
b42.1		b55.1		b68.1	
b42.2		b55.2		b68.2	
b42.3		b55.3		b68.3	
b43.1		b56.1		b69.1	
b43.2		b56.2		b69.2	
b43.3		b56.3		b69.3	
b44.1		b57.1		b70.1	
b44.2		b57.2		b70.2	
b44.3		b57.3		b70.3	
b45.1		b58.1		b71.1	
b45.2		b58.2		b71.2	
b45.3		b58.3		b71.3	
b46.1		b59.1		b72.1	
b46.2		b59.2		b72.2	
b46.3		b59.3		b72.3	
b47.1		b60.1		b73.1	
b47.2		b60.2		b73.2	
b47.3		b60.3		b73.3	
b48.1		b61.1		b74.1	
b48.2		b61.2		b74.2	
b48.3		b61.3		b74.3	
b49.1		b62.1		b75.1	
b49.2		b62.2		b75.2	
b49.3		b62.3		b75.3	
b50.1		b63.1		b76.1	
b50.2		b63.2		b76.2	
b50.3		b63.3		b76.3	
b51.1		b64.1		b77.1	
b51.2		b64.2		b77.2	
b51.3		b64.3		b77.3	
b52.1		b65.1		b78.1	
b52.2		b65.2		b78.2	
b52.3		b65.3		b78.3	

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ᶣ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ᶣ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEᶣ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

1) has the meaning dark for display

Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
b79.1		b92.1		bh5.1	
b79.2		b92.2		bh5.2	
b79.3		b92.3		bh5.3	
b80.1		b93.1		bh6.1	
b80.2		b93.2		bh6.2	
b80.3		b93.3		bh6.3	
b81.1		b94.1		bh7.1	
b81.2		b94.2		bh7.2	
b81.3		b94.3		bh7.3	
b82.1		b95.1		bh8.1	
b82.2		b95.2		bh8.2	
b82.3		b95.3		bh8.3	
b83.1		b96.1		bh9.1	
b83.2		b96.2		bh9.2	
b83.3		b96.3		bh9.3	
b84.1		b97.1			
b84.2		b97.2			
b84.3		b97.3			
b85.1		b98.1			
b85.2		b98.2			
b85.3		b98.3			
b86.1		b99.1			
b86.2		b99.2			
b86.3		b99.3			
b87.1		bh0.1			
b87.2		bh0.2			
b87.3		bh0.3			
b88.1		bh1.1			
b88.2		bh1.2			
b88.3		bh1.3			
b89.1		bh2.1			
b89.2		bh2.2			
b89.3		bh2.3			
b90.1		bh3.1			
b90.2		bh3.2			
b90.3		bh3.3			
b91.1		bh4.1			
b91.2		bh4.2			
b91.3		bh4.3			

Answer cycle

Data source

ncon 1)

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog

AA1.3
AA2.3
AA3.3
AA4.3
AE1A
↓
AE11
Pd01
↓
Pd40
PL01
↓
PL40
SA1.3
↓
S16.3
-1.000
-.500
-.200
-.100
-.050
-.020
-.010
0.000
0.001
0.002
0.005
0.010
0.020
0.050
0.100
0.200
0.500
1.000
1.050
1.100
2.718

digital

AdAP
AE1ᒧ
↓
A11ᒧ
bA1.3
↓
bA4.3
bE01
↓
bE14
Hi
Lo
nAEᒧ
nPAr
nPon
nStr
oPEr
rES1
rES2
SbE1
↓
SbF6
tA1.1
tA1.2
tA1.3
tA1.4
tA1.5
tA1.6
tA1.A
tA1.C
tA1.E
tA1.b
tA1.d
tA1.F
↓
tA5.3
tA5.4
tA5.5
tA5.6
tA5.C
tA5.E
tA5.d
tA5.F
↓
tA7.1
tA7.2
tA7.3
tA7.4
tA7.5
tA7.6
tA7.A
tA7.C
tA7.E
tA7.b
tA7.d
tA7.F
tACt
tAC1
tAC2

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Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
c01.1		c10.4			
c01.2		c11.1		c20.4	
c01.3		c11.2		c21.1	
c01.4		c11.3		c21.2	
c02.1		c11.4		c21.3	
c02.2		c12.1		c21.4	
c02.3		c12.2		c22.1	
c02.4		c12.3		c22.2	
c03.1		c12.4		c22.3	
c03.2		c13.1		c22.4	
c03.3		c13.2		c23.1	
c03.4		c13.3		c23.2	
c04.1		c13.4		c23.3	
c04.2		c14.1		c23.4	
c04.3		c14.2		c24.1	
c04.4		c14.3		c24.2	
c05.1		c14.4		c24.3	
c05.2		c15.1		c24.4	
c05.3		c15.2		c25.1	
c05.4		c15.3		c25.2	
c06.1		c15.4		c25.3	
c06.2		c16.1		c25.4	
c06.3		c16.2		c26.1	
C06.4		c16.3		c26.2	
c07.1		c16.4		c26.3	
c07.2		c17.1		c26.4	
c07.3		c17.2		c27.1	
c07.4		c17.3		c27.2	
c08.1		c17.4		c27.3	
c08.2		c18.1		c27.4	
c08.3		c18.2		c28.1	
c08.4		c18.3		c28.2	
c09.1		c18.4		c28.3	
c09.2		c19.1		c28.4	
c09.3		c19.2		c29.1	
c09.4		c19.3		c29.2	
c10.1		c19.4		c29.3	
c10.2		c20.1		c29.4	
c10.3		c20.2		c30.1	

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ᶣ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ᶣ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEᶣ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

1) has the meaning dark for display

Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
c30.2		d3.01			
c30.3		d3.02			
c30.4		d3.03			
c31.1		d3.04			
c31.2		d3.05			
c31.3		d3.06			
c31.4		d3.07			
c32.1		d3.08			
c32.2		d3.09			
c32.3		d3.10			
c32.3		d3.11			
c33.1		d3.12			
c33.2		d4.01			
c33.3		d4.02			
c33.4		d4.03			
d1.01		d4.04			
d1.02		d4.05			
d1.03		d4.06			
d1.04		d4.07			
d1.05		d4.08			
d1.06		d4.09			
d1.07		d4.10			
d1.08		d4.11			
d1.09		d4.12			
d1.10					
d1.11					
d1.12					
d2.01					
d2.02					
d2.03					
d2.04					
d2.05					
d2.06					
d2.07					
d2.08					
d2.09					
d2.10					
d2.11					
d2.12					

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ᶣ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ᶣ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEᶣ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

1) has the meaning dark for display

Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
h1.01		h3.05		AA4.2	
h1.02		h3.06		AA5.1	
h1.03		h3.07		AA5.2	
h1.04		h3.08		AA6.1	
h1.05		h3.09		AA6.2	
h1.06		h3.10		AA7.1	
h1.07		h3.11		AA7.2	
h1.08		h3.12		AA8.1	
h1.09		h3.13		AA8.2	
h1.10		h3.14		AA9.1	
h1.11		h3.15		AA9.2	
h1.12		h3.16		AAU	
h1.13		h3.17		bA1.1	
h1.14		h3.18		bA1.2	
h1.15		h4.01		ba2.1	
h1.16		h4.02		ba2.2	
h1.17		h4.03		bA3.1	
h1.18		h4.04		bA3.2	
h2.01		h4.05		bA4.1	
h2.02		h4.06		bA4.2	
h2.03		h4.07		bA05	
h2.04		h4.08		bA06	
h2.05		h4.09		bA07	
h2.06		h4.10		bA08	
h2.09		h4.11		bA09	
h2.08		h4.12		bA10	
h2.09		h4.13		bA11	
h2.11		h4.14		bA12	
h2.12		h4.15		bA13	
h2.13		h4.16		bA14	
h2.14		h4.17		bA15	
h2.15		h4.18		bA16	
h2.16		AA1.1		bAU	
h2.17		AA1.2		bSPS	
h2.18		AA2.1		bLS	
h3.01		AA2.2		bLb	
h3.02		AA3.1		dA1.1	
h3.03		AA3.2		dA1.2	
h3.04		AA4.1		dA1.3	

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ᶣ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ᶣ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEᶣ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

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Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data source	Answer dd1 Data sinks	Question dd2 Data sinks	Answer dd1 Data source
dA1.4		L01.1		L07.4	
dA1.M		L01.2		L07.M	
dA1.U		L01.3		L07.U	
dA2.1		L01.4		L08.1	
dA2.2		L01.M		L08.2	
dA2.3		L01–U		L08.3	
dA2.4		L02.1		L08.4	
dA2.M		L02.2		L08.M	
dA2.U		L02.3		L08.U	
dd1.1		L02.4		L09.1	
dd1.2		L02.M		L09.2	
dd1.3		L02.U		L09.3	
dd1.4		L03.1		L09.4	
dd1.M		L03.2		L09.M	
dd1.U		L03.3		L09.U	
dd2.1		L03.4		L10.1	
dd2.2		L03.M		L10.2	
dd2.3		L03.U		L10.3	
dd2.4		L04.1		L10.4	
dd2.M		L04.2		L10.M	
dd2.U		L04.3		L10.U	
dd3.1		L04.4		L11.1	
dd3.2		L04.M		L11.2	
dd3.3		L04.U		L11.3	
dd3.4		L05.1		L11.4	
dd3.M		L05.2		L11.M	
dd3.U		L05.3		L11.U	
		L05.4		L12.1	
		L05.M		L12.2	
		L05.U		L12.3	
		L06.1		L12.4	
		L06.2		L12.M	
		L06.3		L12.U	
		L06.4		L13.1	
		L06.M		L13.2	
		L06.U		L13.3	
		L07.1		L13.4	
		L07.2		L13.M	
		L07.3		L13.U	

Answer cycle

Data source

ncon [1)]

b01.A	c01.A	d1.1A	h1.1A
↓	↓	↓	↓
bh9.A	c33.A	d4.14	h4.4A

analog/digital depending on assignment in FdEF

analog	**digital**	
AA1.3	AdAP	tA5.5
AA2.3	AE1ʟ	tA5.6
AA3.3	↓	tA5.C
AA4.3	A11ʟ	tA5.E
AE1A	bA1.3	tA5.d
↓	↓	tA5.F
AE11	bA4.3	↓
Pd01	bE01	tA7.1
↓	↓	tA7.2
Pd40	bE14	tA7.3
PL01	Hi	tA7.4
↓	Lo	tA7.5
PL40	nAEʟ	tA7.6
SA1.3	nPAr	tA7.A
↓	nPon	tA7.C
S16.3	nStr	tA7.E
-1.000	oPEr	tA7.b
-.500	rES1	tA7.d
-.200	rES2	tA7.F
-.100	SbE1	tACt
-.050	↓	tAC1
-.020	SbF6	tAC2
-.010	tA1.1	
0.000	tA1.2	
0.001	tA1.3	
0.002	tA1.4	
0.005	tA1.5	
0.010	tA1.6	
0.020	tA1.A	
0.050	tA1.C	
0.100	tA1.E	
0.200	tA1.b	
0.500	tA1.d	
1.000	tA1.F	
1.050	↓	
1.100	tA5.3	
2.718	tA5.4	

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Configuring list FCon

Program name:	Processor:	Date:
Customer/system:		Page:

Answer dd1 Data source	Question dd2 Data sinks	Answer dd1 Data source	Question dd2 Data sinks	Question dd2 Data sinks	Answer dd1 Data source	Answer cycle Data source
L14.0		SAA1				ncon [1]
L14.1		SAA2				
L14.2		SAA3				b01.A / c01.A / d1.1A / h1.1A
L14.3		SAA4				↓ / ↓ / ↓ / ↓
L14.4		SAA5				bh9.A / c33.A / d4.14 / h4.4A
L14.5		SAA6				
L14.6		SAA7				analog/digital depending on assignment in FdEF
L14.7		SAA8				**analog** / **digital**
L14.8		SA1.1				AA1.3 / AdAP / tA5.5
L14.9		SA1.2				AA2.3 / AE1↳ / tA5.6
		SA2.1				AA3.3 / ↓ / tA5.C
		SA2.2				**AA4.3** / **A11↳** / **tA5.E**
		SA3.1				AE1A / bA1.3 / tA5.d
		SA3.2				↓ / ↓ / tA5.F
		SA4.1				AE11 / bA4.3 / ↓
		SA4.2				**Pd01** / **bE01** / **tA7.1**
		SA5.1				↓ / ↓ / **tA7.2**
		SA5.2				**Pd40** / **bE14** / **tA7.3**
		SA6.1				PL01 / Hi / tA7.4
		SA6.2				↓ / Lo / tA7.5
		SA7.1				**PL40** / **nAE↳** / **tA7.6**
		SA7.2				**SA1.3** / **nPAr** / **tA7.A**
		SA8.1				↓ / nPon / tA7.C
		SA8.2				S16.3 / nStr / tA7.E
		SbA1				-1.000 / oPEr / tA7.b
		SbA2				**-.500** / **rES1** / **tA7.d**
		SbA3				-.200 / rES2 / tA7.F
		SbA4				-.100 / SbE1 / tACt
		SbA5				-.050 / ↓ / tAC1
		SbA6				**-.020** / **SbF6** / **tAC2**
		SbA7				-.010 / tA1.1
		SbA8				0.000 / tA1.2
		tA1U				0.001 / tA1.3
		tA2U				**0.002** / **tA1.4**
		tA3U				**0.005** / **tA1.5**
		tA4U				0.010 / tA1.6
		tA5U				0.020 / tA1.A
		tA6U				**0.050** / **tA1.C**
		tA7U				**0.100** / **tA1.E**
						0.200 / tA1.b
						0.500 / tA1.d
						1.000 / tA1.F
						1.050 / ↓
						1.100 / tA5.3
						2.718 / tA5.4

[1] has the meaning dark for display

Configuring list FPoS

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Pos. no.	Answer dd1 Function block	Question dd2 Pos. no.	Answer dd1 Function block	Question dd2 Pos. no.	Answer dd1 Function block	Answer cycle d1
n001		n042		n083		nPoS b01.F ↓ bh9.F c01.F ↓ C33.F d01.F ↓ d04.F h01.F h04.F dELt[1] inSt [2] [1] delete [2] insert [1]+[2] only active with Enter key
n002		n043		n084		
n003		n044		n085		
n004		n045		n086		
n005		n046		n087		
n006		n047		n088		
n007		n048		n089		
n008		n049		n090		
n009		n050		n091		
n010		n051		n092		
n011		n052		n093		
n012		n053		n094		
n013		n054		n095		
n014		n055		n096		
n015		n056		n097		
n016		n057		n098		
n017		n058		n099		
n018		n059		n100		
n019		n060		n101		
n020		n061		n102		
n021		n062		n103		
n022		n063		n104		
n023		n064		n105		
n024		n065		n106		
n025		n066		n107		
n026		n067		n108		
n027		n068		n109		
n028		n069		n110		
n029		n070		n111		
n030		n071		n112		
n031		n072		n113		
n032		n073		n114		
n033		n074		n115		
n034		n075		n116		
n035		n076		n117		
n036		n07		n118		
n037		n078		n119		
n038		n079		n120		
n039		n080		n121		
n040		n081		n122		
n041		n082		n123		

- Arithmetic blocks identified by ndEF in FdEF do not appear in the answer cycle
- already positioned blocks do not appear in the answer cycle

Configuring list FPoS

Program name:	Processor:	Date:
Customer/system:		Page:

Question dd2 Pos. no.	Answer dd1 Function block	Question dd2 Pos. no.	Answer dd1 Function block	Question dd2 Pos. no.	Answer dd1 Function block	Answer cycle d1
n124		n165				nPoS b01.F ↓ bh9.F c01.F ↓ C33.F d01.F ↓ d04.F h01.F h04.F dELt[1] inSt [2] [1] delete [2] insert [1]+[2] only active with Enter key
n125		n166				
n126		n167				
n127		n168				
n128		n169				
n129		n170				
n130		n171				
n131		n172				
n132		n173				
n133		n174				
n134		n175				
n135						
n136						
n137						
n138						
n139						
n140						
n141						
n142						
n143						
n144						
n145						
n146						
n147						
n148						
n149						
n150						
n151						
n152						
n153						
n154						
n155						
n156						
n157						
n158						
n159						
n160						
n161						
n162						
n163						
n164						

- Arithmetic blocks identified by ndEF in FdEF do not appear in the answer cycle
- already positioned blocks do not appear in the answer cycle

Configuring list oFPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
dA1.1	dA	0.0		%	dd3.2	dP	_ _ _		–
	dE	100.0		%		dA	0.0		–
dA1.2	dA	0.0		%		dE	100.0		–
	dE	100.0		%	dd3.3	dP	_ _ _		–
dA1.3	dA	0.0		%		dA	0.0		–
	dE	100.0		%		dE	100.0		–
dA1.4	dA	0.0		%	dd3.4	dP	_ _ _		–
	dE	100.0		%		dA	0.0		–
dA2.1	dA	0.0		%		dE	100.0		–
	dE	100.0		%	Cnt1	StP	4		–
dA2.2	dA	0.0		%	CPt1	PA	1.000		1
	dE	100.0		%		PE	1.000		1
dA2.3	dA	0.0		%		tA	1.000		1
	dE	100.0		%		tE	1.000		1
dA2.4	dA	0.0		%	CPt2	PA	1.000		1
	dE	100.0		–		PE	1.000		1
dd2.1	dP	_ _ _ . –		–		tA	1.000		1
	dA	0.0		–		tE	1.000		1
	dE	100.0		–					
dd2.2	dP	_ _ _ . –		–					
	dA	0.0		–					
	dE	100.0		–					
dd2.3	dP	_ _ _ . –		–					
	dA	0.0		–					
	dE	100.0		–					
dd2.4	dP	_ _ _ . –		–					
	dA	0.0		–					
	dE	100.0		–					
dd3.1	dP	_ _ _		–					
	dA	0.0		–					
	dE	100.0		–					

Configuring list oFPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
FUL1	0	0.0		%	FUP2	–10	–10.0		%
	20	20.0		%		0	0.0		%
	40	40.0		%		10	10.0		%
	60	60.0		%		20	20.0		%
	80	80.0		%		30	30.0		%
	100	100.0		%		40	40.0		%
FUL2	0	0.0		%		50	50.0		%
	20	20.0		%		60	60.0		%
	40	40.0		%		70	70.0		%
	60	60.0		%		80	80.0		%
	80	80.0		%		90	90.0		%
	100	100.0		%		100	100.0		%
FUL3	0	0.0		%		110	110.0		%
	20	20.0		%					
	40	40.0		%	MUP1	StP	8		–
	60	60.0		%	MUP2	StP	8		–
	80	80.0		%	SES	bdr	9600		baud
	100	100.0		%		Lrc	norM		–
FUP1	–10	–10.0		%		LET	noL		–
	0	0.0		%		Prt	EvEn		–
	10	10.0		%		Snr	0		–
	20	20.0		%		Cbt	OFF		–
	30	30.0		%					
	40	40.0		%					
	50	50.0		%					
	60	60.0		%					
	70	70.0		%					
	80	80.0		%					
	90	90.0		%					
	100	100.0		%					
	110	110.0		%					

Configuring list CLPA

Program name:	Processor:	Date:
Customer/system:		Page:

CLFo: CLCy: CLSb: CLPr:

Interval/ Program	CLTi	CLA1	CLA2	Clb1	Clb2	Clb3	Clb4	Clb5	Clb6	Clb7	Clb8

Configuring list onPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
dd.1.1	dr	1		1)	Pd21	–	10.00		1
dd.1.2	dr	1		1)	Pd22	–	10.00		1
dd.1.3	dr	1		1)	Pd23	–	10.00		1
dd.1.4	dr	1		1)	Pd24	–	10.00		1
dd.2.1	dr	1		1)	Pd25	–	10.00		1
dd2.2	dr	1		1)	Pd26	–	10.00		1
dd2.3	dr	1		1)	Pd27	–	10.00		1
dd2.4	dr	1		1)	Pd28	–	10.00		1
dd.3.1	dr	1		1)	Pd29	–	10.00		1
dd.3.2	dr	1		1)	Pd30	–	10.00		1
dd3.3	dr	1		1)	Pd31	–	10.00		1
dd.3.4	dr	1		1)	Pd32	–	10.00		1
Pd10	–	10.00		1	Pd33	–	10.00		1
Pd02	–	10.00		1	Pd34	–	10.00		1
Pd03	–	10.00		1	Pd35	–	10.00		1
Pd04	–	10.00		1	Pd36	–	10.00		1
Pd05	–	10.00		1	Pd37	–	10.00		1
Pd06	–	10.00		1	Pd38	–	10.00		1
Pd07	–	10.00		1	Pd39	–	10.00		1
Pd08	–	10.00		1	Pd40	–	10.00		1
Pd09	–	10.00		1	PL01	–	0.000		1
Pd10	–	10.00		1	PL02	–	0.000		1
Pd11	–	10.00		1	PL03	–	0.000		1
Pd12	–	10.00		1	PL04	–	0.000		1
Pd13	–	10.00		1	PL05	–	0.000		1
Pd14	–	10.00		1	PL06	–	0.000		1
Pd15	–	10.00		1	PL07	–	0.000		1
Pd16	–	10.00		1	PL08	–	0.000		1
Pd17	–	10.00		1	PL09	–	0.000		1
Pd18	-	10.00		1	PL10	–	0.000		1
Pd19	–	10.00		1	PL11	–	0.000		1
Pd20	–	10.00		1	PL12	–	0.000		1

Configuring list onPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
PL13	–	0.000		1		tr	oFF		(s)
PL14	–	0.000		1		LiA	–5.0		%
PL15	–	0.000		1		LiE	105.0		%
PL16	–	0.000		1	Ain2	tin	10.00		(s)
PL17	–	0.000		1		tr	oFF		(s)
PL18	–	0.000		1		LiA	–5.0		%
PL19	–	0.000		1		LiE	105.0		%
PL20	–	0.000		1	bin1	tin	ProG		(s)
PL21	–	0.000		1		tr	oFF		(s)
PL22	–	0.000		1		LiA	–5.0		%
PL23	–	0.000		1		LiE	105.0		%
PL24	–	0.000		1	bin2	tin	ProG		(s)
PL25	–	0.000		1		tr	oFF		(s)
PL26	–	0.000		1		LiA	–5.0		%
PL27	–	0.000		1		LiE	105.0		%
PL28	–	0.000		1	bin3	tin	ProG		(s)
PL29	–	0.000		1		tr	oFF		(s)
PL30	–	0.000		1		LiA	–5.0		%
PL31	–	0.000		1		LiE	105.0		%
PL32	–	0.000		1	bin4	tin	ProG		(s)
PL33	–	0.000		1		tr	oFF		(s)
PL34	–	0.000		1		LiA	–5.0		%
PL35	–	0.000		1		LiE	105.0		%
PL36	–	0.000		1	bin5	tin	ProG		(s)
PL37	–	0.000		1		tr	oFF		(s)
PL38	–	0.000		1		LiA	–5.0		%
PL39	–	0.000		1		LiE	105.0		%
PL40	–	0.000		1	bin6	tin	ProG		(s)
AFi1	tF	1.000		s		tr	oFF		(s)
AFi2	tF	1.000		s		LiA	–5.0		%
Ain1	tin	10.00		s		LiE	105.0		%

Configuring list onPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
Ccn1	cP	0.100		1		Yo	AUto		(%)
	tn	9984		s		YA	–5.0		%
	tv	oFF		(s)		YE	105.0		%
	vv	5.0		1		tY	60		s
	AH	0.0		%	CSE1	cP	0.100		1
	Yo	AUto		(%)		tn	9984		s
	YA	–5.0		%		tv	oFF		(s)
	YE	105.0		%		vv	5.0		1
	tY	60		s		AH	0.0		%
Ccn2	cP	0.100		1		Yo	AUto		(%)
	tn	9984		s		YA	–5.0		%
	tv	oFF		(s)		YE	105.0		%
	vv	5.0		1		ty	60		s
	AH	0.0		%		tA	180		ms
	Yo	AUto		(%)		tE	180		ms
	YA	–5.0		%	CSE2	CP	0.100		1
	YE	105.0		%		tn	9984		s
	tY	60		s		tv	oFF		(s)
Ccn3	cP	0.100		1		vv	5.0		1
	tn	9984		s		AH	0.0		%
	tv	oFF		(s)		Yo	AUto		(%)
	vv	5.0		1		YA	–5.0		%
	AH	0.0		%		YE	105.0		%
	Yo	AUto		(%)		ty	60		s
	YA	–5.0		%		tA	180		ms
	YE	105.0		%		tE	180		ms
	tY	60		s					
Ccn4	cP	0.100		1					
	tn	9984		s					
	tv	oFF		(s)					
	vv	5.0		1					
	AH	0.0		%					

Configuring list onPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
CSE3	cP	0.100		1		tv	oFF		(s)
	tn	9984		s		vv	5.0		1
	tv	oFF		(s)		AH	0.0		%
	vv	5.0		1		ty	60		s
	AH	0.0		%		tA	180		ms
	Yo	AUto		(%)		tE	180		ms
	YA	–5.0		%	CSi3	cP	0.100		1
	YE	105.0		%		tn	9984		s
	ty	60		s		tv	oFF		(s)
	tA	180		ms		vv	5.0		1
	tE	180		ms		AH	0.0		%
CSE4	cP	0.100		1		ty	60		s
	tn	9984		s		tA	180		ms
	tv	oFF		(s)		tE	180		ms
	vv	5.0		1	CSi4	cP	0.100		1
	AH	0.0		%		tn	9984		s
	Yo	AUto		(%)		tv	oFF		(s)
	YA	–5.0		%		vv	5.0		1
	YE	105.0		%		AH	0.0		%
	ty	60		s		ty	60		s
	tA	180		ms		tA	180		ms
	tE	180		ms		tE	180		ms
CSi1	cP	0.100		1	dti1	td	1		s
	tn	9984		s	dti2	td	1		s
	tv	oFF		(s)					
	vv	5.0		1					
	AH	0.0		%					
	ty	60		s					
	tA	180		ms					
	tE	180		ms					
CSi2	cP	0.100		1					
	tn	9984		s					

Configuring list onPA

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name		Value dd1		Dimen-sion	Parameter name		Value dd1		Dimen-sion
dd2	dd3	Factory setting	Customer setting		dd2	dd3	Factory setting	Customer setting	
SPr1	SPA	0.0		%					
	SPE	100.0		%					
SPr2	SPA	0.0		%					
	SPE	100.0		%					
SPr3	SPA	0.0		%					
	SPE	100.0		%					
SPr4	SPA	0.0		%					
	SPE	100.0		%					
SPr5	SPA	0.0		%					
	SPE	100.0		%					
SPr6	SPA	0.0		%					
	SPE	100.0		%					
SPr7	SPA	0.0		%					
	SPE	100.0		%					
Spr8	SPA	0.0		%					
	SPE	100.0		%					
PUM1	tAE	20		ms					
	tM	0.1		s					
PUM2	tAE	20		ms					
	tM	0.1		s					
PUM3	tAE	20		ms					
	tM	0.1		s					
PUM4	tAE	20		ms					
	tM	0.1		s					
tAC1	PEr								
	tA5								
tAC2	PEr								
	tA5								

CAE4/5 Parameters

Program name:	Processor:	Date:
Customer/system:		Page:

Parameter name	Value		Dimension	CAE4 CAE5
	Factory setting	Customer setting		
dd2	dd1	dd1		dd3
SenS	Mv.			
unit	°C			
t_C	L			
t_B	50.0			
Mr	10.00			
Cr	–			
M_P	_ _ _ . –			
M_A	0.0			
M_E	100.0			
C_A				
C_E				
PC				

9 List of Abbreviations

AA*	Analog outputs 1 to 4
AA*.1, AA*.2	Analog outputs (sinks)
AA*.3	Analog outputs (sources)
AAU	Analog output switch
AbS	Absolute value (b)
AdAP	Parameterization mode Adaptation
AdAP	Data source adaptation status
Add	Adder (b)
AE*	Analog inputs 1 to 8
AEFr	Mains frequency suppression of the the analog inputs
AE*A	Analog inputs 1 to 8 (sources)
AE* ↳	Fault message source of AE1 to 8
AFi*	Adaptive filters 1 to 8 (c)
AH	Response threshold (dead zone)
Ain	Integrator with analog input 1, 2 (c)
AL	“Adaptation in progress” (source)
AMEM	Analog value memory (b)
AMPL	Amplifier (b)
And	AND function (b)
APSt	Configuring mode (all preset) factory setting
APST MEM	Error message factory setting
ASo	Analog switch over (b)
AUto	automatic
AU	Preselection input adaptation

b**.A	Arithmetic block b01 to b85, output (source)
b**.F	Arithmetic block b01 to b85, function assignment
b**.*	Arithmetic block b01 to b85, input 1 to 3 (sink)
bAtt	Battery backup
bAU	Digital output switch
bA*.*	DIgital output 1 to 4 (sink 1, 2)
bA*.3	Digital output 1 to 4 (source)
bA**	Digital output 05 to 16 (sink)
bdr	SES: Baud rate
bA**	Digital input 01 to 14 (source)
bin*	Integrator with digital input 1, 2 (c)
bLb	Digital input; blocking operation
bLPS	Digital input; blocking parameterization, configuring
bLS	DIgital input; blocking configuring
bSo	Digital switch over (b)

c**.A	Arithmetic block c01 to c15, output (source)
c**.F	Arithmetic block c01 to c15, function assignment
c**.*	Arithmetic block c01 to c15, input 1 to 3 (sink)
CAEx	Parameter for UNI module
Cbt	Parameter: Watchdog SES
Ccn*	K–controller 1, 2 (h)
CLA*	Analog output 1, 2 of the clock

CLb*	Digital output 1 to 8 of the clock
CLCY	Parameter: Number of cycles of the programs (Cloc)
CLFo	Parameter: Clock format (Cloc)
CLoc	Clock (d)
CLPA	Paramterization preselection mode: Clock parameter
CLPr	Parameter: Number of intervals (Cloc)
CLSb	Parameter: Fast clock (Cloc)
CLti	Parameter: Interval time (Cloc)
CMPL	Longitudinal parity formation Lrc complement
CMPt – Err	Compatibility error between customer program and operating software
Cnt	Demultiplexer
CoMP	Comparator (b)
CoUn	Counter (b)
CP	K_p, Proportional action factor (controller)
CPt*	Correction computer 1, 2 (c)
CPU.-Err	Error message CPU (Slave Processor)
CPU-Err	Error message CPU
CSE*	S-controller 1, 2; external position feedback signal (h)
CSi*	S-controller 1, 2; internal position feedback signal (h)
CYCL	cyclic

d0*.F	Arithmetic block d01 to d03, function assignment
d**.*	Arithmetic block d1 to d3, input 01 to 12 (sink)
d*.*A	Arithmetic block d1 to d3, output 1 to 9 (source)
d*.**.	Arithmetic block d1 to d3, output 10 to 14 (source)
dA	Parameter, Start (display range)
dA–L	Display selection, analog display LEDs (hdEF)
dA*	Analog display 1, 2
dA*.*	Analog display 1, 2; Input 1, 2 (sink)
dA*.U	Analog display 1, 2; switching (sink)
dd*	Digital display 1, 2, 3
dd*.*	Digital display 1 to 3; Input 1, 2 (sink)
dd*.U	Digital display 1 to 3, switching (sink)
dE	Parameter, End (display range)
dEbA	Response threshold (dead band) (b)
dEF	define
dELt	delete
dFF	D flip–flop (b)
diF	Differentiator (b)
div	Divider (b)
dP	Decimal point (display dd1 to dd3)
dPon	Flashing of dd1 to dd3 after Pon (hdEF)
dPv	Parameter: Adaptation step direction
dr	Repetition rate (displays)
dti*	Dead time element 1, 2 (dead-time) (c)
dY	Parameter: Adaptation step height

Eor	Exor (b)
Err	Error

Et–L	Longitudinal parity with Lrc after ETX
EuEn	Cross parity formation even
FASt	fast
FCon	Configuring mode: Wiring function
FdEF	Configuring mode: Define function
Filt	Filter (low pass) (b)
FPoS	Configuring mode: Function positioning
FUL*	Function transmitter 1 to 3 (c)
FUP*	Function transmitter 1,2 with rounding (c)
h	hour
H	Manual mode
h0*.F	Arithmetic block h01, h02, function assignment
h*.**	Arithmetic block h1, 2 inputs 01 to 18 (sinks)
h*.*A	Arithmetic block h1, 2, output 1 to 4 (source)
hdEF	Parameterization preselection mode (define hardware)
Hi	High, logic 1
inSt	insert, insert in pos. row
Kp	Proportional action factor
L**.*	LEDs L01 to L13, Inputs 1, 2 (sink)
L**.U	LEDs L01 to L13, Input switching
L14.*	LEDs L14.0 to L14.9 (sink)
LED	LED (light emitting diode)
LEt	Longitudinal parity position SES
L–Et	Longitudinal parity position before ETX
LG	Decadic logarithmer
LiA	Parameter: Limit Start
LiE	Parameter: Limit End
LiMi	Limiter (b)
LinE	linear equation (b)
Ln	Natural logarithmer (b)
Lo	Low, logic 0
Lrc	Longitudinal parity formation SES
MAME	Maximum-Memory (b)
MASE	Maximum selection (b)
MEM	Memory (b)
MiME	Minimum-Memory (b)
MiSE	Minimum selection (b)
ModE	Operating mode
MULt	Multiplier (b)

MUP*	Measuring point multiplexer analog (d)
N	Trace, digital signal
n***	Number of positioning No. 001 to 129
nAE ↳	Message signal: no MU fault
nAME	Name (id of the user program memory)
nAnd	NAND (b)
ncon	not connected
ndEF	not defined
no	no
no L	Longitudinal parity SES without Lrc
noP	no operation
nor	NOR (b)
norM	Longitudinal parity formation Lrc normal
not	none
nPAr	no parameterization
nPon	no power on
nPoS	not positioned
nStr	no structuring
odd	vertical parity formation odd
oFF	off
oFL	Overflow positive
oFL, –oFL	Overflow negative
oFPA	Offline parameter
onPA	Online parameter
oP**	Error message: Option 5, 6
or	OR (b)
ovEr Shot	Error message: overshoot
P	P–operation
PA	Parameter: Start value
Pd**	Logarithmic parameters 01 to 16
PE	Parameter: full scale
Pi	PI controller structure
Pid	PID controller structure
PL**	Linear parameters 01 to 29
PoFF MEM	Error message customer memory contents
–PoS	Positioning error
Pot	Exponential function (b)
ProG	Progressive
Prt	Vertical parity
PS	Parameterization/Configuring
Pv oFL	Error message: Range overshoot
PUM	Pulse width modulator

root	root (b)
SA*.1	SES: Analog input 1 to 8, UN (sink, analog)
SA*.2	SES: Analog input 1 to 8, N (sink, digital)
SA*.3	SES: Analog input 1 to 8 (source)
SAA*	SES: Analog output 1 to 8 (sink)
SbA*	SES: Digital output 1 to 8 (sink)
SbE*	SES: Digital input 1 to 8 (source)
SES	Serial interface
SG*	Controlling variable 1 to 3
SMAL	Error message: small
Snr	SES station number
StAt	static
StP	Switch steps
SUb	Subtractor (b)
tA	Parameter: Start of scale
tA*.*	Key tA1 to tA7, output 1 to 6 (source)
tA*.U	Key tA1 to tA7, switching (sink, digital)
tAE	Minimum turn–on time
tACt	Clock signal (source)
td	Parameter dead time
tE	Parameter: Full scale
tESt	Test
tF	Filter time constant
tFF	T-flip-flop (b)
TG	Delay time of the controlled system
tiME	Timer, monoflop (b)
tin	Integration time
tM	Period
tn	Integral action time
tS	Parameter setpoint ramp
to	to
tr	Tracking time
tU	Monitoring time
tv	Derivative action time
tY	Actuating time
vv	Derivation gain
x	Controlled variable
xdD	Control difference D–element
xdI	Control difference I–element
xdP	Control difference P–element
xdS	Control difference position controller
y	Manipulated variable

yA	Manipulated variable start
ya	Automatic manipulated variable
ya	Manipulated variable in non–automatic mode
± YBL	Blocking signal for manipulated variable
yE	Manipulated variable full scale
YES	yes
$yI(t)$	I-part of the manipulated variable at time t
$yI\|_{t=0}$	Working point of the I-part at time t = 0
Yo	Working point P–controller (manipulated variable)
YH	Manual manipulated variable
y_L	Last manipulated variable before power failure
YN	Tracking variable
y_p	P-part of the manipulated variable
YR	Position feedback variable
YZ	Disturbance variable to the output (manipulated variable)

$\pm\Delta w$	incremental w–adjustment
$\pm\Delta y$	incremental y adjustment

0MA	0 mA, constant current
4MA	4 mA, constant current
50H	50 Hz Frequency suppression
60H	60 Hz Frequency suppression
5BE	Option module 5 digital inputs
4BA	Option module 4 digital inputs
2rEL	Option module 2 relays
3AE	Option module 3 analog inputs
1AA	Option module 1 analog output (yHold)
*.n	New parameter
*.o	Old parameter
↯	Fault

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